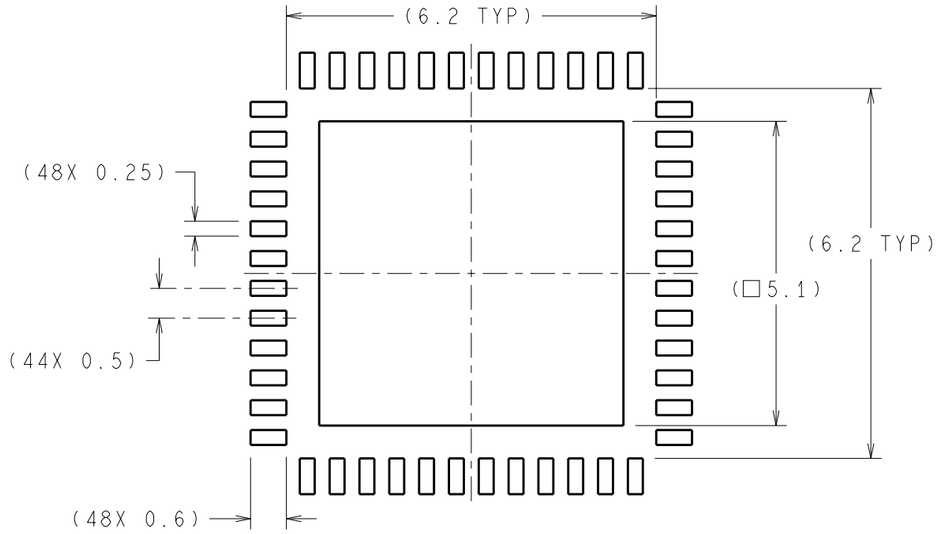
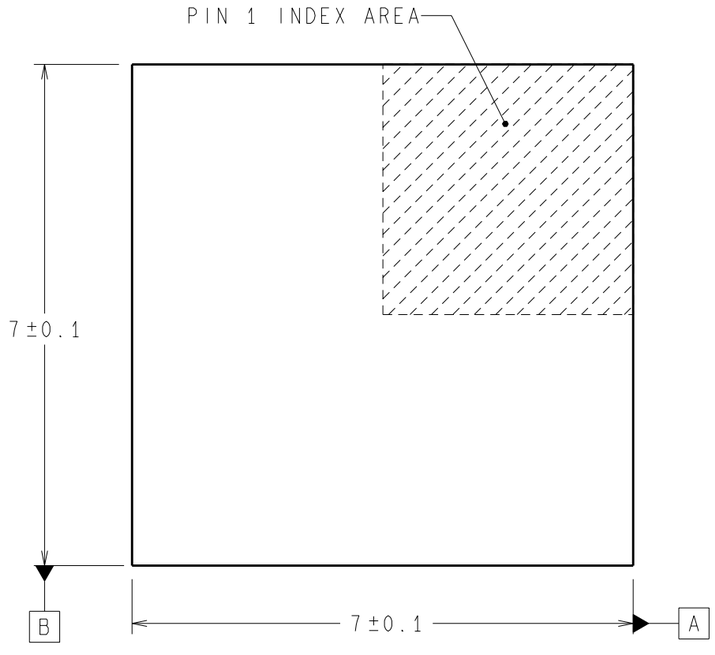
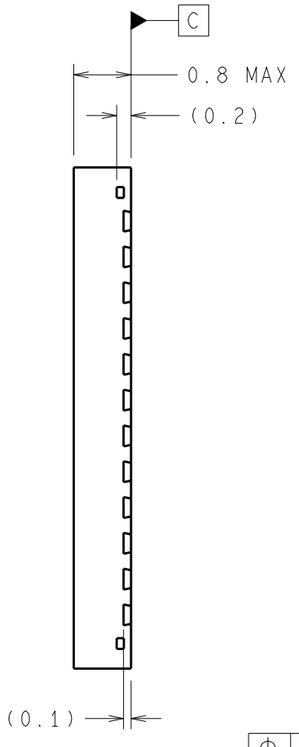
REVISIONS				
REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	1012	05/06/2003	LY/TL/SN

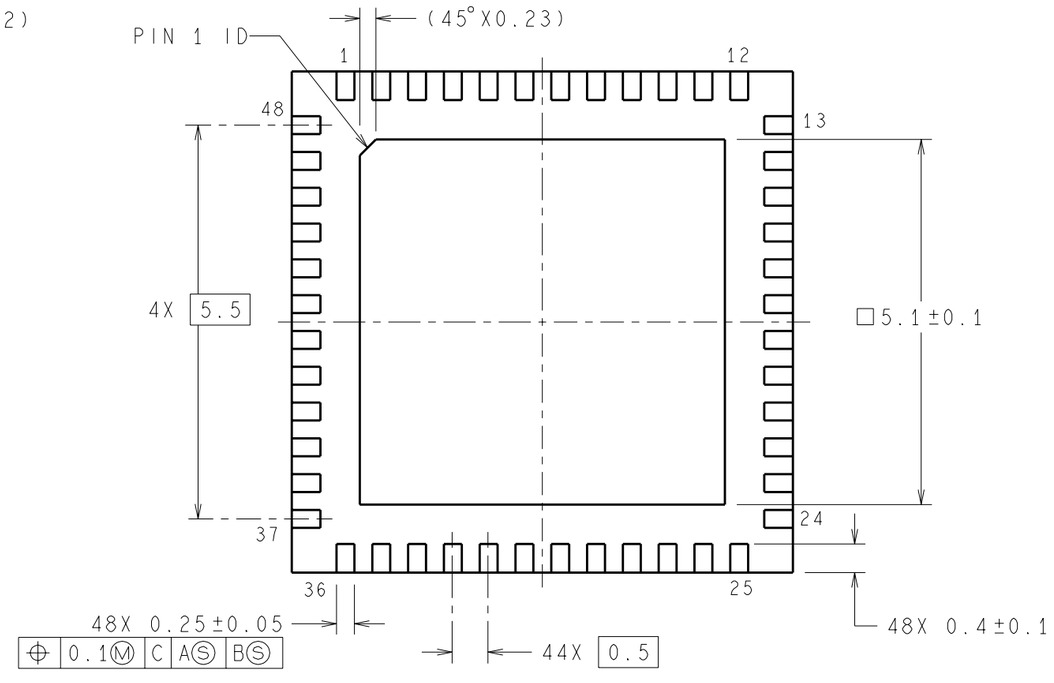


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS







NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR SOLDER THICKNESS AND COMPOSITION, SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. MAXIMUM ALLOWABLE METAL BURR ON LEAD TIPS AT THE PACKAGE EDGES IS 76 MICRONS.
3. REFERENCE JEDEC REGISTRATION MO-220, VARIATION WKKD-2.

APPROVALS	DATE
DRAWN: LYE MENG KONG	05/06/2003
DFTG. CHK.: THANH LEQUANG	05/06/2003
ENGR. CHK.: N. SANTHIRAN	05/06/2003

PROJECTION: MM

National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95052-8090

LLP, PLASTIC, QUAD, 7x7x0.8mm BODY, 48 LD, 0.5mm PITCH, NO PULLBACK

SCALE	SIZE	DRAWING NUMBER	REV
NTS	B	(SC)MKT-SQA48A	A

FORMERLY: N/A

SHEET 1 of 1