Fully Accurate, 12-/14-/16-Bit V_{OUT} *nano*DAC, Quad, SPI Interface, 4.5 V to 5.5 V in TSSOP

AD5024/AD5044/AD5064

FEATURES

- Low power quad 12-/14-/16-bit DAC, ±1 LSB INL
- Pin compatible and performance upgrade to AD5666
- Individual and common voltage reference pin options
- Rail-to-rail operation
- 4.5 V to 5.5 V power supply
- Power-on reset to zero scale or midscale
- 3 power-down functions and per-channel power-down
- Hardware $\overline{LDAC}$ with software $\overline{LDAC}$ override function
- $\overline{CLR}$ function to programmable code
- SDO daisy-chaining option
- 14-/16-lead TSSOP
- Internal reference buffer and internal output amplifier

APPLICATIONS

- Process control
- Data acquisition systems
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators

FUNCTIONAL BLOCK DIAGRAMS

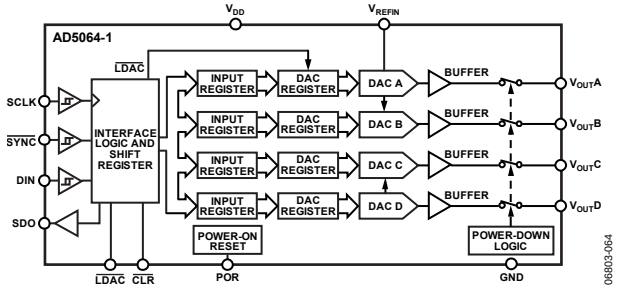

Figure 1. AD5064-1 Functional Equivalent and Pin Compatible with AD5666

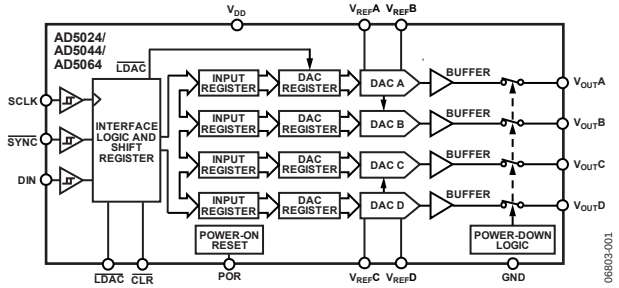

Figure 2. AD5024/AD5044/AD5064 with Individual Reference Pins

GENERAL DESCRIPTION

The AD5024/AD5044/AD5064/AD5064-1 are low power, quad 12-/14-/16-bit buffered voltage output *nano*DAC® converters that offer relative accuracy specifications of 1 LSB INL and 1 LSB DNL with the AD5024/AD5044/AD5064 individual reference pin and the AD5064-1 common reference pin options. The AD5024/AD5044/AD5064/AD5064-1 can operate from a single 4.5 V to 5.5 V supply. The AD5024/AD5044/AD5064/AD5064-1 also offer a differential accuracy specification of ±1 LSB. The parts use a versatile 3-wire, low power Schmitt trigger serial interface that operates at clock rates up to 50 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, and DSP interface standards. Integrated reference buffers and output amplifiers are also provided on-chip. The AD5024/AD5044/AD5064/AD5064-1 incorporate a power-on reset circuit that ensures the DAC output powers up to zero scale or midscale and remains there until a valid write takes place to the device. The AD5024/AD5044/AD5064/AD5064-1 contain a power-down feature that reduces the current consumption of the device to typically 400 nA at 5 V and provides software selectable output loads while in power-down mode. Total unadjusted error for the parts is <2 mV.

PRODUCT HIGHLIGHTS

1. Quad channel available in 14-/16-lead TSSOP packages.
2. 16-bit accurate, 1 LSB INL.
3. High speed serial interface with clock speeds up to 50 MHz.
4. Reset to known output voltage (zero scale or midscale).

Table 1. Related Devices

Part No.	Description
AD5666	Quad,16-bit buffered DAC, 16 LSB INL, TSSOP
AD5025/AD5045/AD5065	Dual, 16-bit buffered DACs, 1 LSB INL, TSSOP
AD5062, AD5063	16-bit *nano*DAC, 1 LSB INL, SOT-23, MSOP
AD5061	16-bit *nano*DAC, 4 LSB INL, SOT-23
AD5040/AD5060	14-/16-bit *nano*DAC, 1 LSB INL, SOT-23

Rev. B

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SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V, R_L = 5 kΩ to GND, C_L = 200 pF to GND, 2.5 V ≤ V_{REFIN} ≤ V_{DD}, unless otherwise specified. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	B Grade[1]			A Grade[1, 2]				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
STATIC PERFORMANCE[3]								
Resolution	16			16			Bits	AD5064/AD5064-1
	14						Bits	AD5044
	12						Bits	AD5024
Relative Accuracy (INL)[4]		±0.5	±1		±0.5	±4	LSB	AD5064/AD5064-1; T_A = −40°C to +105°C
		±0.5	±2		±0.5	±4	LSB	AD5064/AD5064-1; T_A = −40°C to +125°C
		±0.25	±1				LSB	AD5044
		±0.12	±0.5				LSB	AD5024
Differential Nonlinearity (DNL)[4]		±0.2	±1		±0.2	±1	LSB	
Total Unadjusted Error			±2			±2	mV	V_{REF} = 2.5 V, V_{DD} = 5.5 V
Offset Error[4, 5]		±0.2	±1.8		±0.2	±1.8	mV	
Offset Error Temperature Coefficient[4, 6]		±2			±2		µV/°C	
Full-Scale Error[4]		±0.01	±0.07		±0.01	±0.07	% FSR	All 1s loaded to DAC register, $V_{REF} < V_{DD}$
Gain Error[4]		±0.005	±0.05		±0.005	±0.05	% FSR	$V_{REF} < V_{DD}$
Gain Temperature Coefficient[4, 6]		±1			±1		ppm FSR/°C	
DC Crosstalk[4, 6]			40			40	µV	Due to single-channel, full-scale output change, R_L = 5 kΩ to GND or V_{DD}
			40			40	µV/mA	Due to load current change
			40			40	µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[6]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability			1			1	nF	R_L = 5 kΩ, R_L =100 kΩ, and R_L = ∞
DC Output Impedance								
Normal Mode		0.5			0.5		Ω	
Power-Down Mode								
Output Connected to 100 kΩ Network		100			100		kΩ	Output impedance tolerance ± 20 kΩ
Output Connected to 1 kΩ Network		1			1		kΩ	Output impedance tolerance ± 400 Ω
Short-Circuit Current		60			60		mA	DAC = full scale, output shorted to GND
		45			45		mA	DAC = zero scale, output shorted to V_{DD}
Power-Up Time[7]		4.5			4.5		µs	
DC PSRR		−92			−92		dB	V_{DD} ± 10%, DAC = full scale, $V_{REF} < V_{DD}$
REFERENCE INPUTS								
Reference Input Range	2.2		V_{DD}	2.2		V_{DD}	V	
Reference Current		35	50		35	50	µA	Per DAC channel; individual reference option
		140	160		140	160	µA	Single reference option
Reference Input Impedance		120			120		kΩ	Individual reference option
		32			32		kΩ	Single reference option
LOGIC INPUTS								
Input Current[8]			±1			±1	µA	
Input Low Voltage, V_{INL}			0.8			0.8	V	
Input High Voltage, V_{INH}	2.2			2.2			V	
Pin Capacitance[6]		4			4		pF	

Parameter	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	A Grade[1, 2] Min	A Grade[1, 2] Typ	A Grade[1, 2] Max	Unit	Conditions/Comments
LOGIC OUTPUTS (SDO)[9]								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} − 1			V_{DD} − 1				I_{SOURCE} = 2 mA
High Impedance Leakage Current		±0.002	±1		±0.002	±1	µA	
High Impedance Output Capacitance[6]		7			7		pF	
POWER REQUIREMENTS								
V_{DD}	4.5		5.5	4.5		5.5	V	DAC active, excludes load current
I_{DD}[10]								$V_{IH} = V_{DD}$, V_{IL} = GND, Code = midscale
Normal Mode		4	6		4	6	mA	
All Power-Down Modes[11]		0.4	2		0.4	2	µA	T_A = −40°C to +105°C
			30			30	µA	T_A = −40°C to +125°C

[1] Temperature range is −40°C to +125°C, typical at 25°C.
[2] A grade offered in AD5064 only.
[3] Linearity and total unadjusted error are calculated using a reduced code range—AD5064/AD5064-1: Code 512 to Code 65,024; AD5044: Code 128 to Code 16,256; AD5024: Code 32 to Code 4064. Output unloaded.
[4] See the Terminology section.
[5] Offset error calculated using a reduced code range—AD5064/AD5064-1: Code 512 to Code 65,024; AD5044: Code 128 to Code 16,256; AD5024: Code 32 to Code 4064. Output unloaded
[6] Guaranteed by design and characterization; not production tested.
[7] Time to exit power-down mode to normal mode; 32nd clock edge to 90% of DAC midscale value, output unloaded.
[8] Current flowing into individual digital pins. V_{DD} = 5.5 V; V_{REF} = 4.096 V; Code = midscale.
[9] AD5064-1 only.
[10] Interface inactive. All DACs active. DAC outputs unloaded.
[11] All four DACs powered down.

AC CHARACTERISTICS

V_{DD} = 4.5 V to 5.5 V, R_L = 5 kΩ to GND, C_L = 200 pF to GND, 2.5 V ≤ V_{REFIN} ≤ V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time		5.8	8	µs	¼ to ¾ scale and ¾ to ¼ scale settling to ±1 LSB, R_L = 5 kΩ, single-channel update
		10.7	13	µs	¼ to ¾ scale and ¾ to ¼ scale settling to ±1 LSB, R_L = 5 kΩ, all channel update
Slew Rate		1.5		V/µs	
Digital-to-Analog Glitch Impulse		3		nV-sec	1 LSB change around major carry
Reference Feedthrough		−90		dB	V_{REF} = 3 V ± 0.86 V p-p, frequency = 100 Hz to 100 kHz
Digital Feedthrough		0.1		nV-sec	
Digital Crosstalk		1.9		nV-sec	
Analog Crosstalk		2		nV-sec	
DAC-to-DAC Crosstalk		3.5		nV-sec	
AC Crosstalk		6		nV-sec	
Multiplying Bandwidth		340		kHz	V_{REF} = 3 V ± 0.86 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 3 V ± 0.2 V p-p, frequency = 10 kHz
Output Noise Spectral Density		64		nV/√Hz	DAC code = 0x8400, frequency = 1 kHz
		60		nV/√Hz	DAC code = 0x8400, frequency = 10 kHz
Output Noise		6		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +125°C, typical at 25°C.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 4 and Figure 5. V_{DD} = 4.5 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
SCLK Cycle Time	t_1	20			ns
SCLK High Time	t_2	10			ns
SCLK Low Time	t_3	10			ns
$\overline{SYNC}$ to SCLK Falling Edge Setup Time	t_4	17			ns
Data Setup Time	t_5	5			ns
Data Hold Time	t_6	5			ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7	5		30	ns
Minimum $\overline{SYNC}$ High Time (Single Channel Update)	t_8	2			µs
Minimum $\overline{SYNC}$ High Time (All Channel Update)	t_8	8			µs
$\overline{SYNC}$ Rising Edge to SCLK Fall Ignore	t_9	17			ns
$\overline{LDAC}$ Pulse Width Low	t_{10}	20			ns
SCLK Falling Edge to $\overline{LDAC}$ Rising Edge	t_{11}	20			ns
$\overline{CLR}$ Minimum Pulse Width Low	t_{12}	10			ns
SCLK Falling Edge to $\overline{LDAC}$ Falling Edge	t_{13}	10			ns
$\overline{CLR}$ Pulse Activation Time	t_{14}	10.6			µs
SCLK Rising Edge to SDO Valid	t_{15}[2, 3]			22	ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_{16}[2]	5			ns
$\overline{SYNC}$ Rising Edge to SCLK Rising Edge	t_{17}[2]	8			ns
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$/$\overline{CLR}$/$\overline{PDL}$ Falling Edge (Single Channel Update)	t_{18}[2]	2			µs
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$/$\overline{CLR}$/$\overline{PDL}$ Falling Edge (All Channel Update)	t_{18}[2]	8			µs
$\overline{PDL}$ Minimum Pulse Width Low	t_{19}	20			ns
Power-up Time[4]		4.5			µs

[1] Maximum SCLK frequency is 50 MHz at V_{DD} = 4.5 V to 5.5 V. Guaranteed by design and characterization; not production tested.
[2] Daisy-chain mode only.
[3] Measured with the load circuit of Figure 3. t_{15} determines the maximum SCLK frequency in daisy-chain mode. AD5064-1 only.
[4] Time to exit power-down mode to normal mode of AD5024/AD5044/AD5064/AD5064-1, 32nd clock edge to 90% of DAC midscale value, with output unloaded.

Circuit and Timing Diagrams

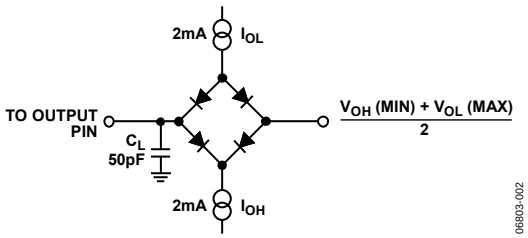

Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

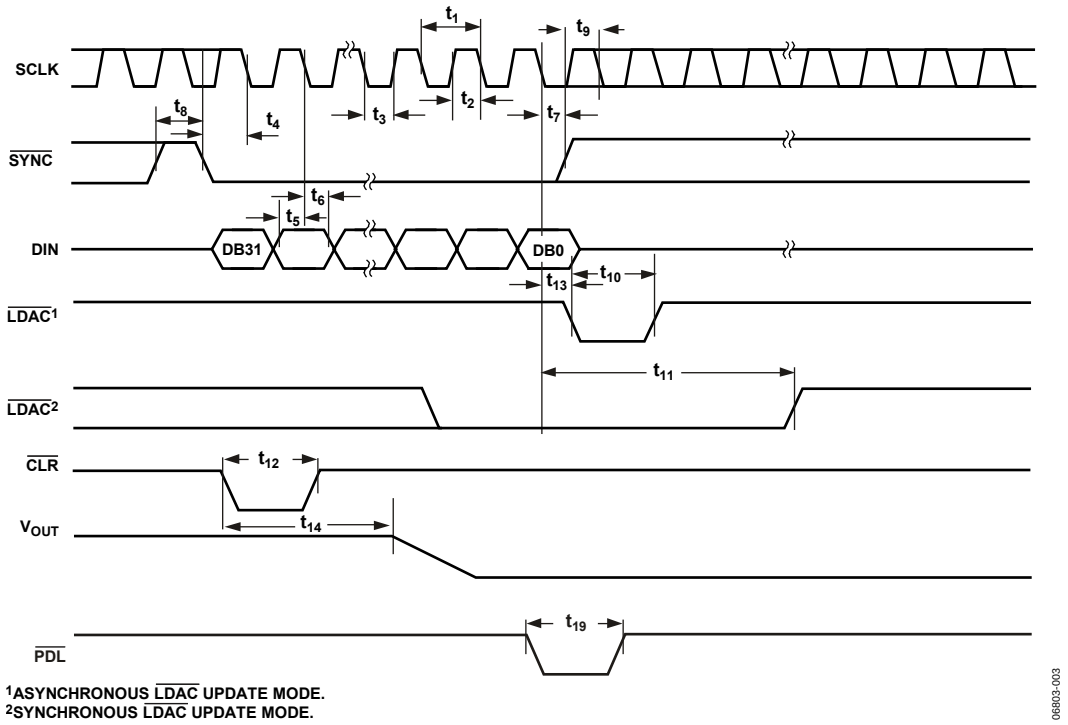

Figure 4. Serial Write Operation

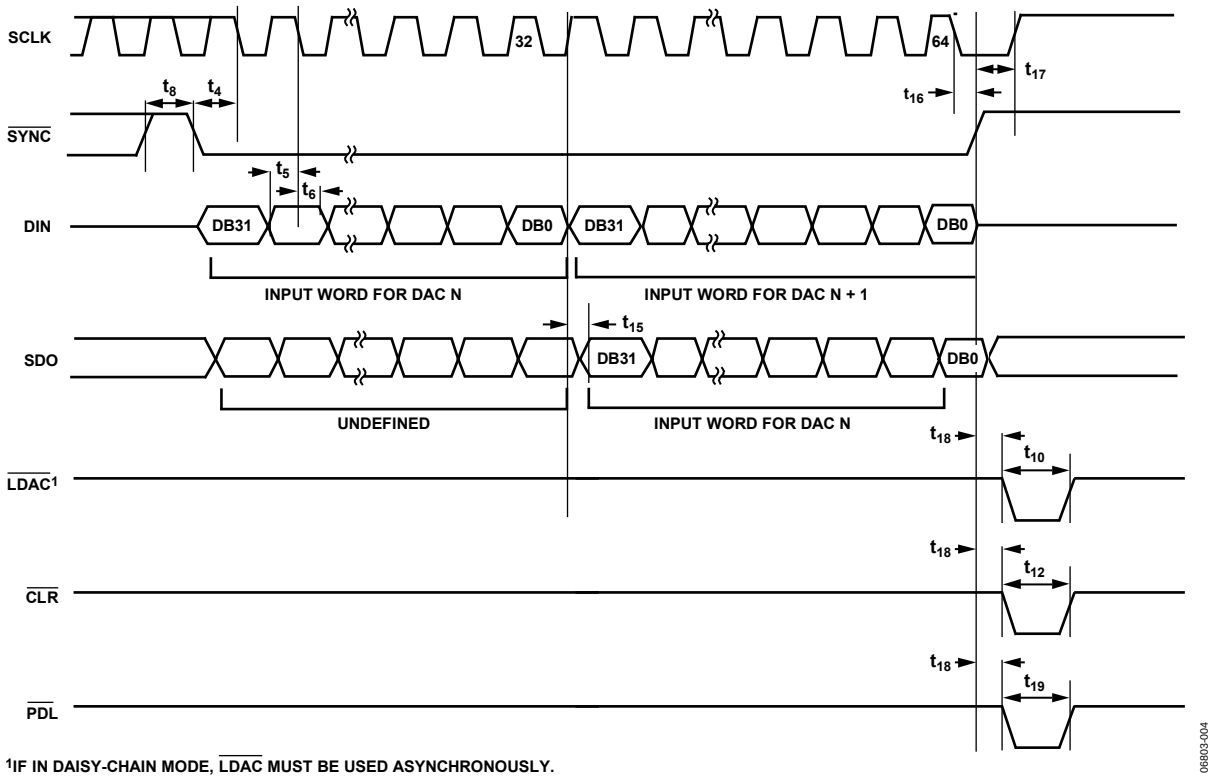

Figure 5. Daisy-Chain Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	150°C
TSSOP Package	
Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	113°C/W
Reflow Soldering Peak Temperature	
Pb-Free	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

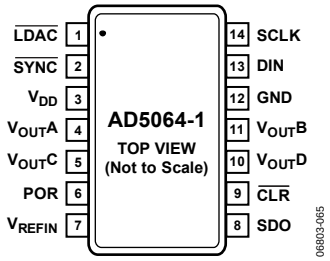

Figure 6. 14-Lead TSSOP (RU-14)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	$\overline{\text{LDAC}}$ can be operated in two modes, asynchronously and synchronously, as shown in Figure 4. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. This pin can also be tied permanently low in standalone mode. When daisy-chain mode is enabled, this pin cannot be tied permanently low; the $\overline{\text{LDAC}}$ pin should be used in asynchronous $\overline{\text{LDAC}}$ update mode, as shown in Figure 5, and the $\overline{\text{LDAC}}$ pin must be brought high after pulsing.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. These parts can be operated from 4.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
5	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	POR	Power-On Reset Pin. Tying this pin to GND powers up all four DACs to zero scale. Tying this pin to V_{DD} powers up all four DACs to midscale.
7	V_{REFIN}	This is a common pin for reference input for DAC A, DAC B, DAC C, and DAC D.
8	SDO	Serial Data Output. Can be used to daisy-chain a number of AD5064-1 devices together. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
9	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the clear code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
10	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
11	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
12	GND	Ground Reference Point for All Circuitry on the Part.
13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the shift register on the falling edge of the serial clock input.
14	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

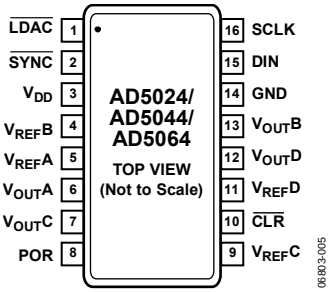

Figure 7. 16-Lead TSSOP (RU-16) Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	$\overline{\text{LDAC}}$ can be operated in two modes, asynchronously and synchronously, as shown in Figure 4. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. This pin can also be tied permanently low in standalone mode.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. These parts can be operated from 4.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	$V_{REF}B$	DAC B Reference Input. This is the reference voltage input pin for DAC B.
5	$V_{REF}A$	DAC A Reference Input. This is the reference voltage input pin for DAC A.
6	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
7	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
8	POR	Power-On Reset. Tying this pin to GND powers up the part to 0 V. Tying this pin to V_{DD} powers up the part to midscale.
9	$V_{REF}C$	DAC C Reference Input. This is the reference voltage input pin for DAC C.
10	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the clear code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
11	$V_{REF}D$	DAC D Reference Input. This is the reference voltage input pin for DAC D.
12	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
13	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
14	GND	Ground Reference Point for All Circuitry on the Part.
15	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the shift register on the falling edge of the serial clock input.
16	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

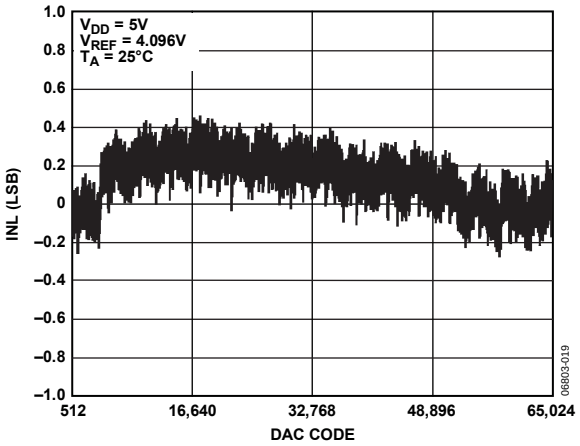

Figure 8. AD5064/AD5064-1 INL

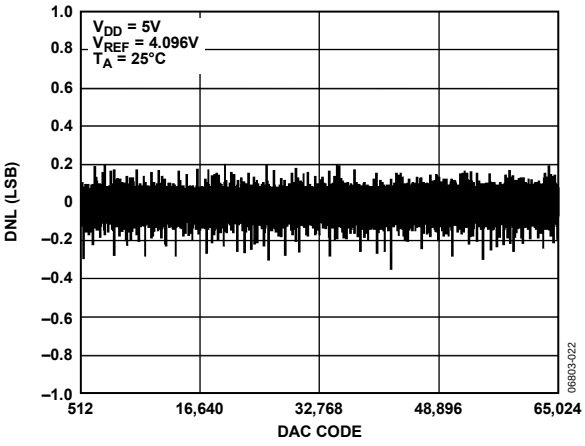

Figure 11. AD5064/AD5064-1 DNL

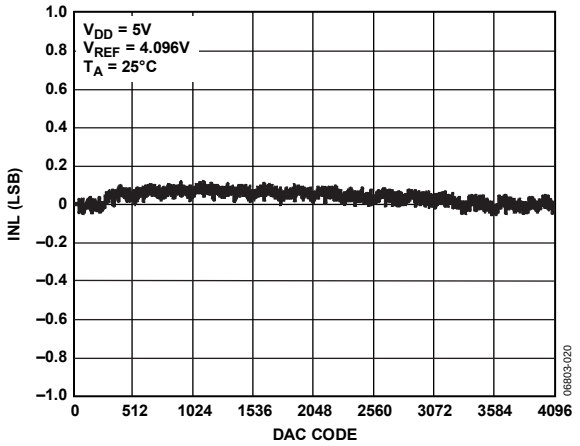

Figure 9. AD5044 INL

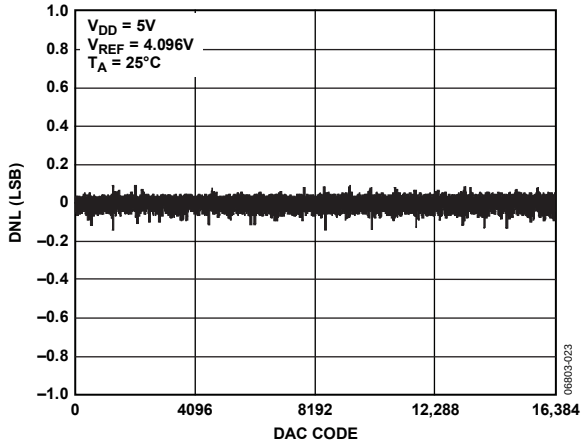

Figure 12. AD5044 DNL

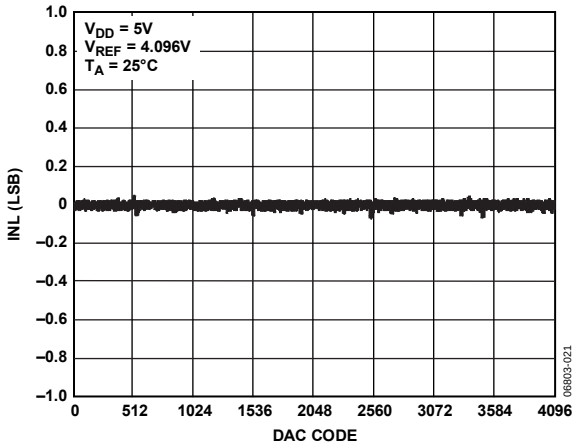

Figure 10. AD5024 INL

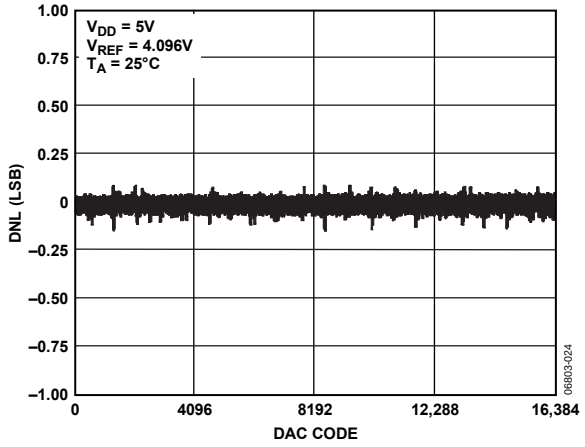

Figure 13. AD5024 DNL

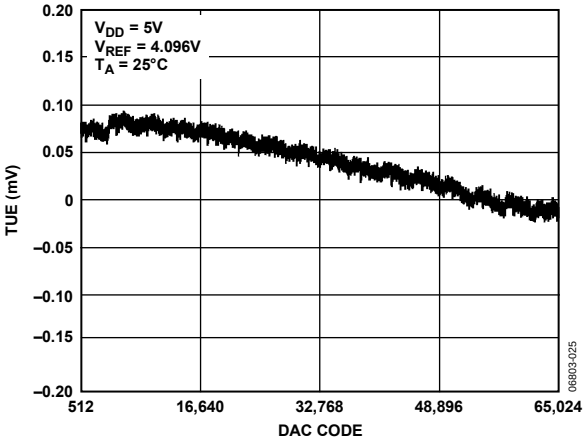

Figure 14. Total Unadjusted Error (TUE)

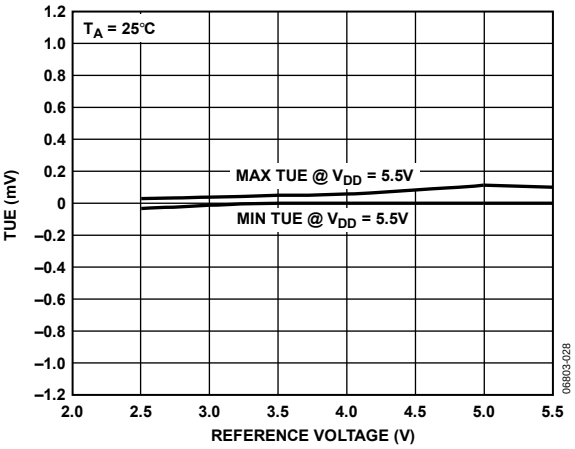

Figure 17. TUE vs. Reference Input Voltage

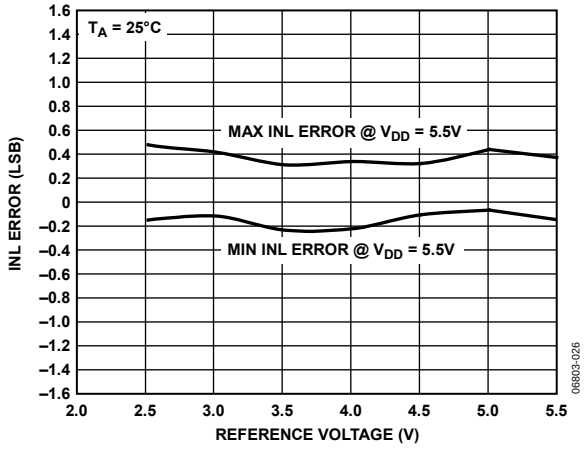

Figure 15. INL vs. Reference Input Voltage

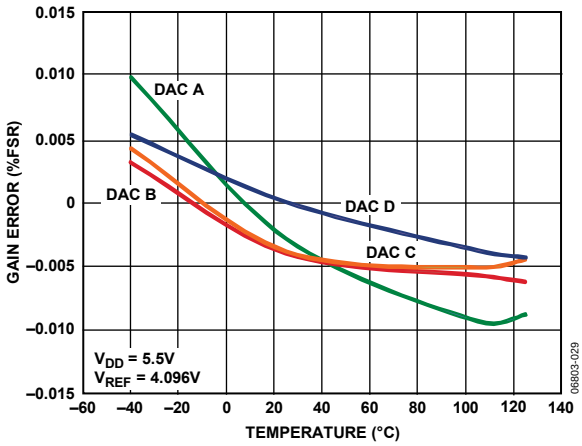

Figure 18. Gain Error vs. Temperature

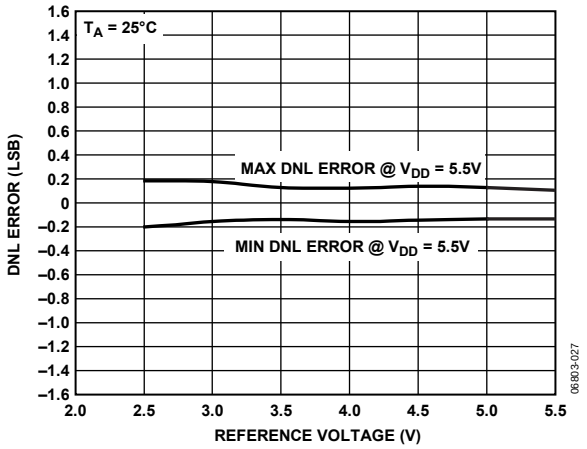

Figure 16. DNL vs. Reference Input Voltage

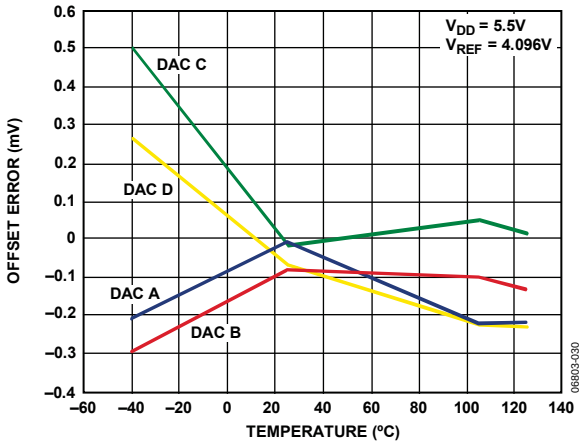

Figure 19. Offset Error vs. Temperature

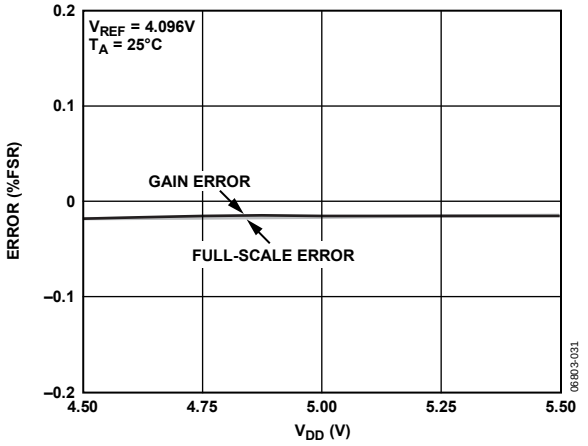

Figure 20. Gain Error and Full-Scale Error vs. Supply Voltage

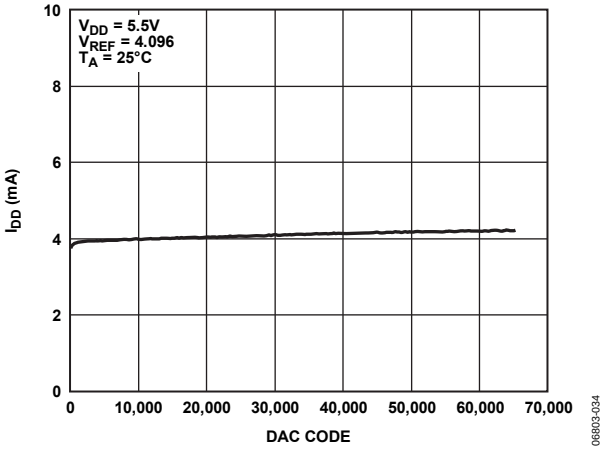

Figure 23. Supply Current vs. Code

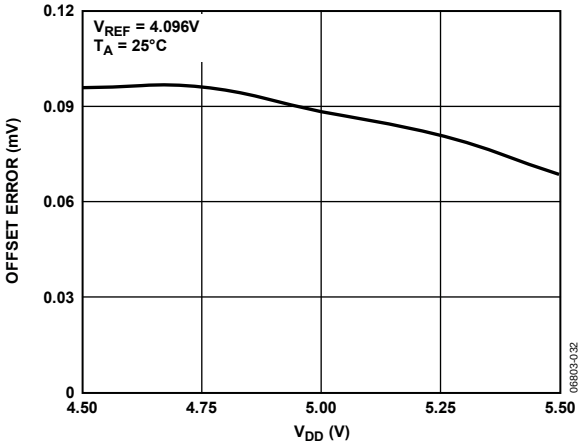

Figure 21. Offset Error Voltage vs. Supply Voltage

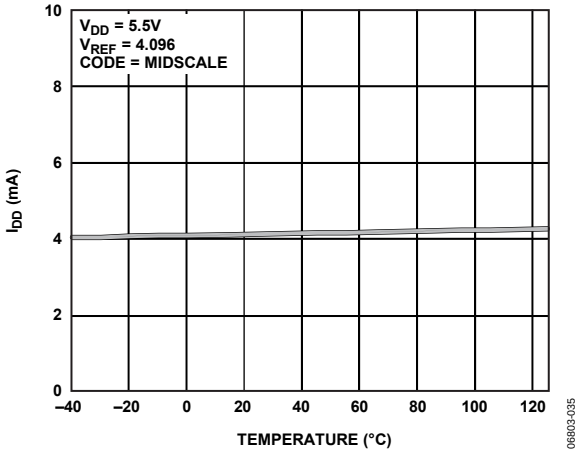

Figure 24. Supply Current vs. Temperature

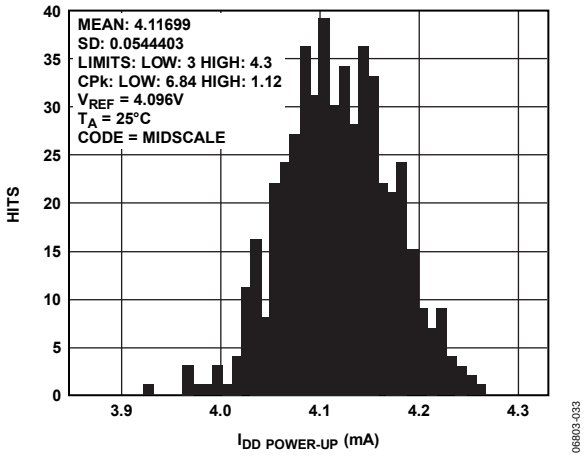

Figure 22. I_{DD} Histogram, V_{DD} = 5.0 V

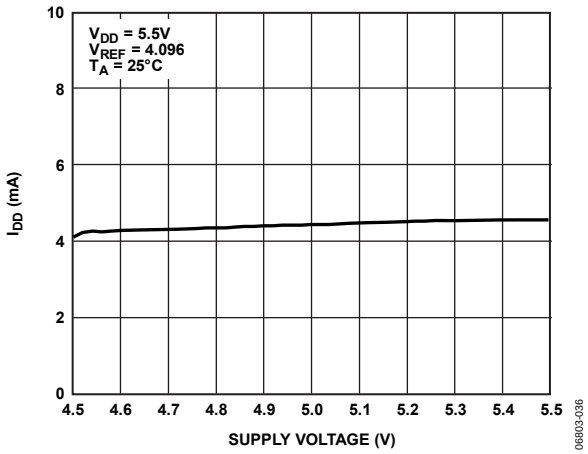

Figure 25. Supply Current vs. Supply Voltage

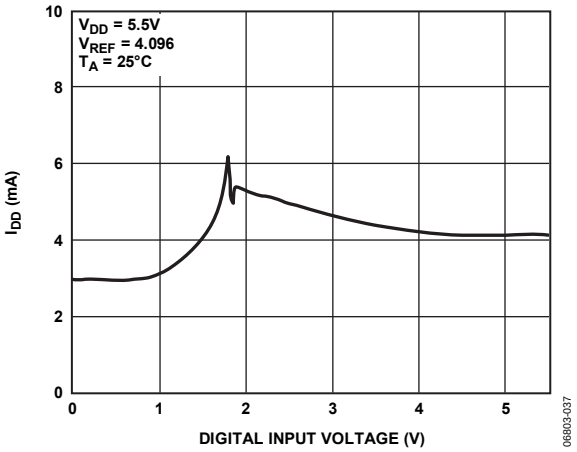

Figure 26. Supply Current vs. Digital Input Voltage

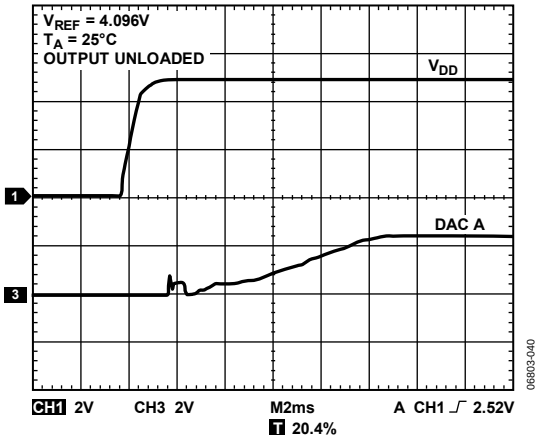

Figure 29. Power-On Reset to Midscale

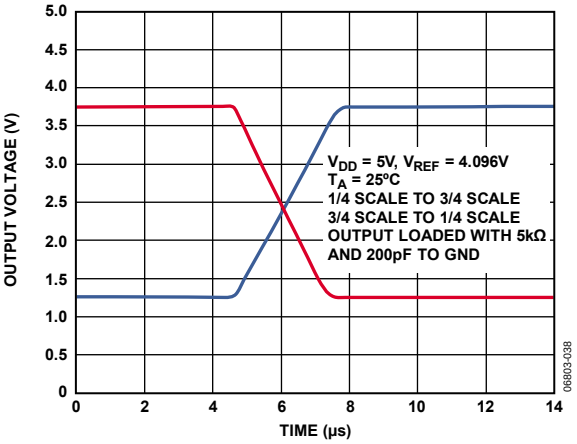

Figure 27. Settling Time

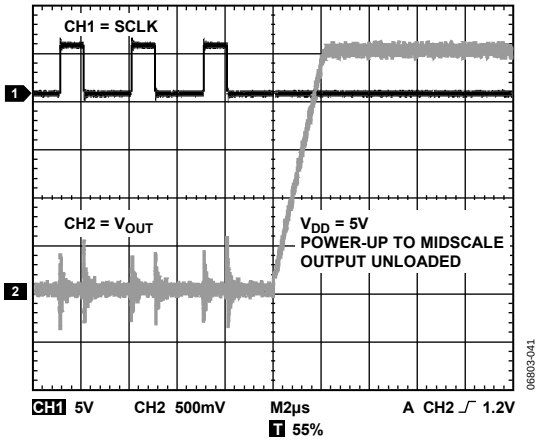

Figure 30. Exiting Power-Down to Midscale

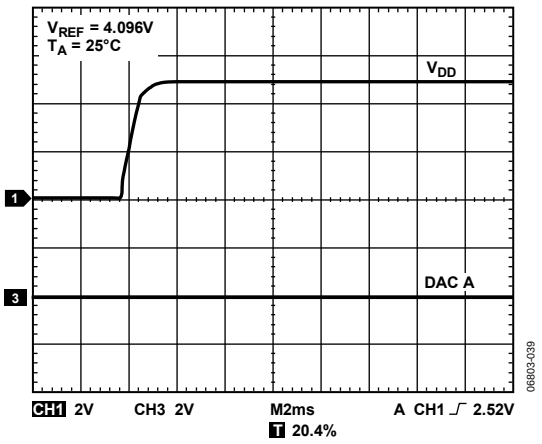

Figure 28. Power-On Reset to 0 V

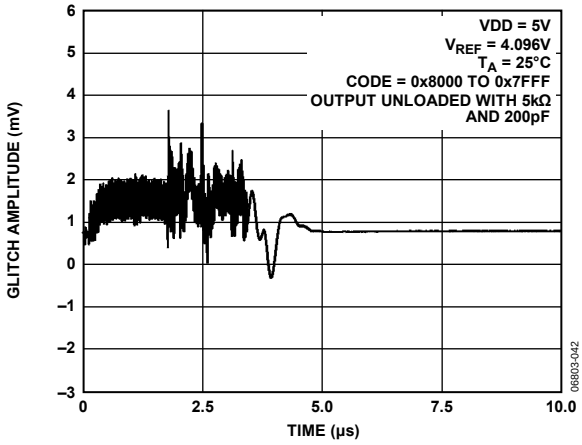

Figure 31. Digital-to-Analog Glitch Impulse

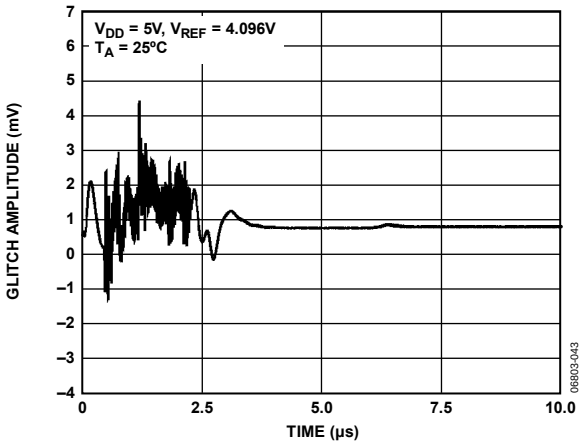

Figure 32. Analog Crosstalk

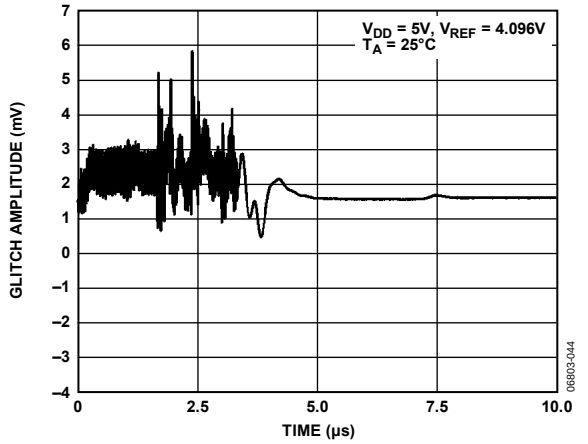

Figure 33. DAC-to-DAC Crosstalk

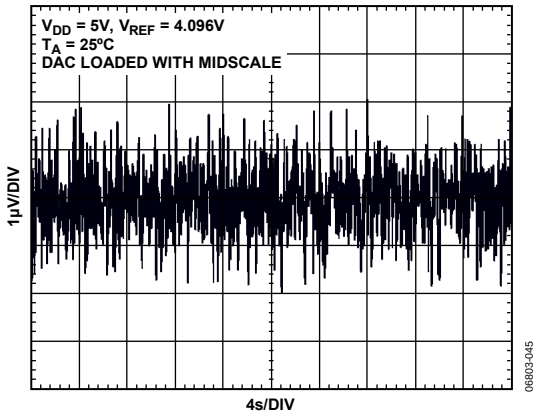

Figure 34. 0.1 Hz to 10 Hz Output Noise Plot

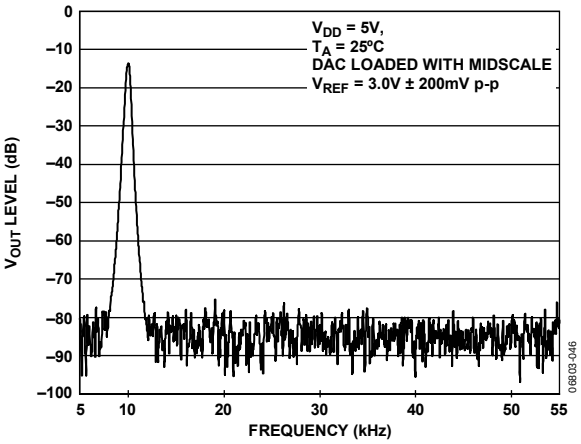

Figure 35. Total Harmonic Distortion

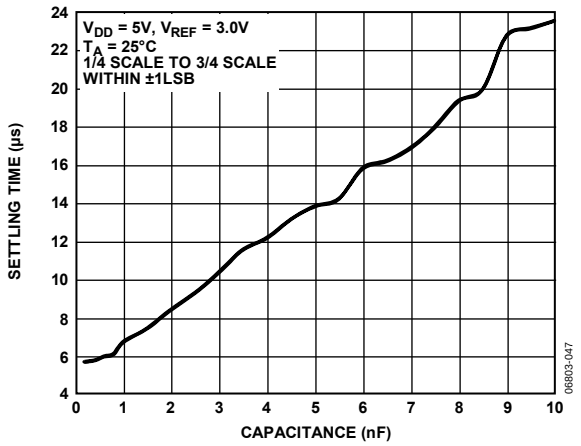

Figure 36. Settling Time vs. Capacitive Load

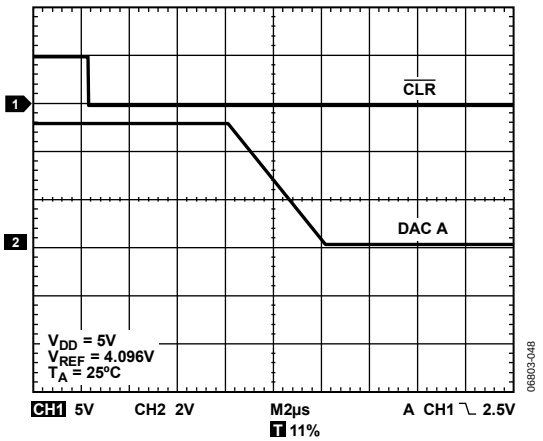

Figure 37. Hardware $\overline{CLR}$

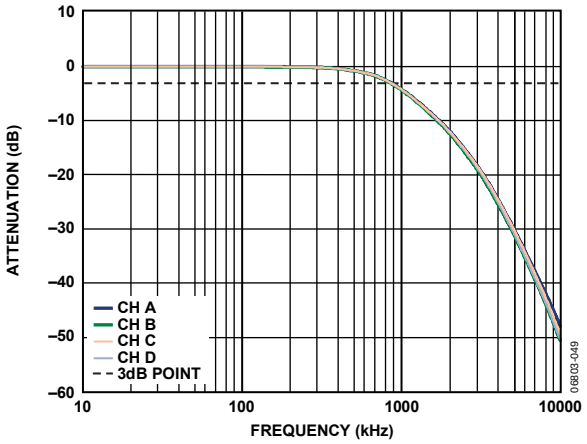

Figure 38. Multiplying Bandwidth

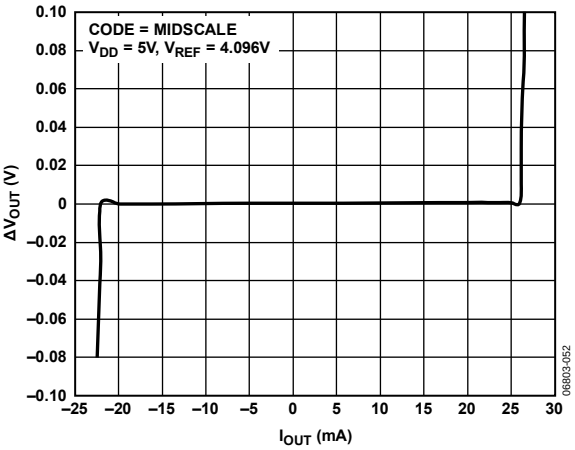

Figure 41. Typical Current Limiting Plot

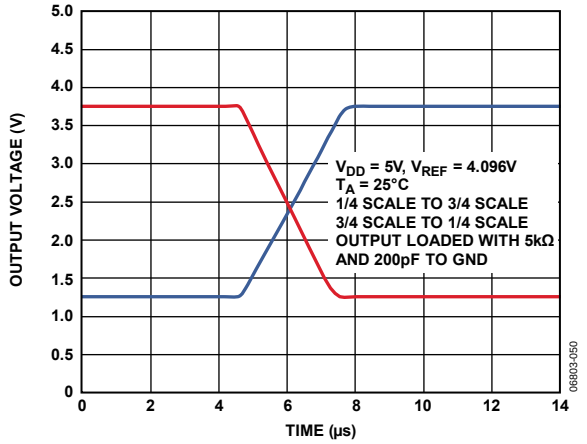

Figure 39. Typical Output Slew Rate

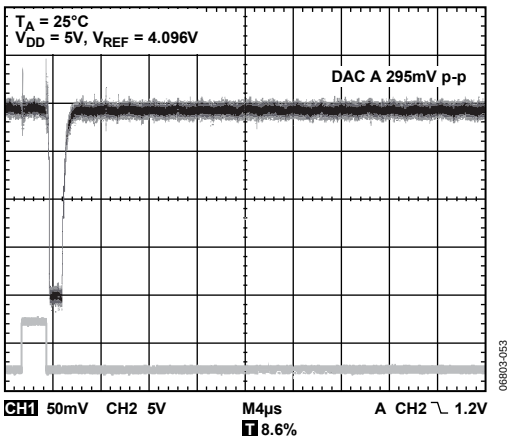

Figure 42. Glitch Upon Entering Power-Down (1 kΩ to GND) from Zero Scale, No Load

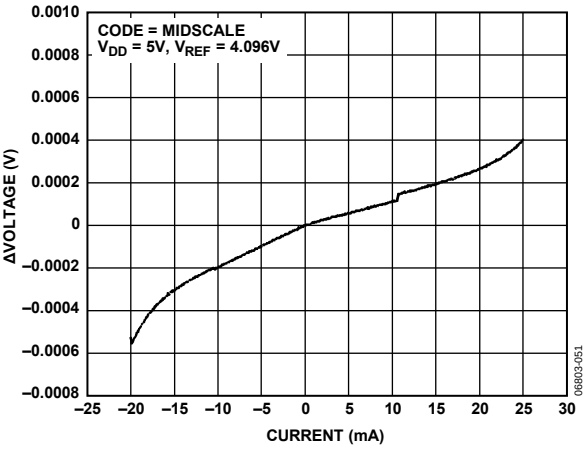

Figure 40. Typical Output Load Regulation

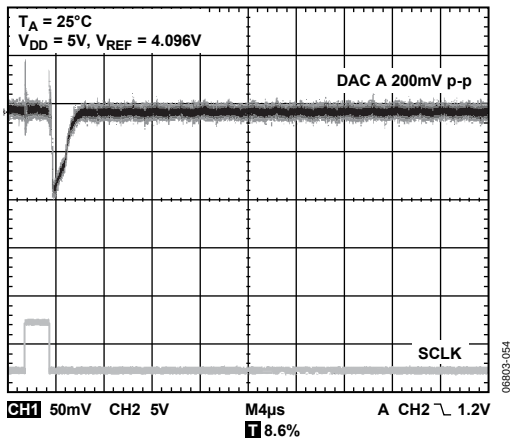

Figure 43. Glitch Upon Entering Power-Down (1 kΩ to GND) from Zero Scale, 5 kΩ/200 pF Load