Features

- **Operating Range from 5V to 27V**
- **Baud Rate up to 20Kbaud**
- **LIN Physical Layer According to LIN Specification 2.0, 2.1 and SAEJ2602-2**
- **Fully Compatible with 3.3V and 5V Devices**
- **TXD Dominant Timeout Timer**
- **Normal and Sleep Mode**
- **Wake-up Capability via LIN Bus (90µs Dominant)**
- **Very Low Standby Current During Sleep Mode (10µA)**
- **Bus Pin is Overtemperature and Short-circuit Protected Versus GND and Battery**
- **LIN Input Current < 2µA if VBAT Is Disconnected**
- **Overtemperature Protection**
- **High EMC Level**
- **Interference and Damage Protection According to ISO/CD 7637**
- **Fulfills the OEM Hardware Requirements for LIN in Automotive Applications Rev. 1.1**
- **Transceiver 2: Additional INH High Side Switch Output and High Voltage WAKE Input**

Dual LIN Transceiver

Atmel ATA6670

Preliminary

1. Description

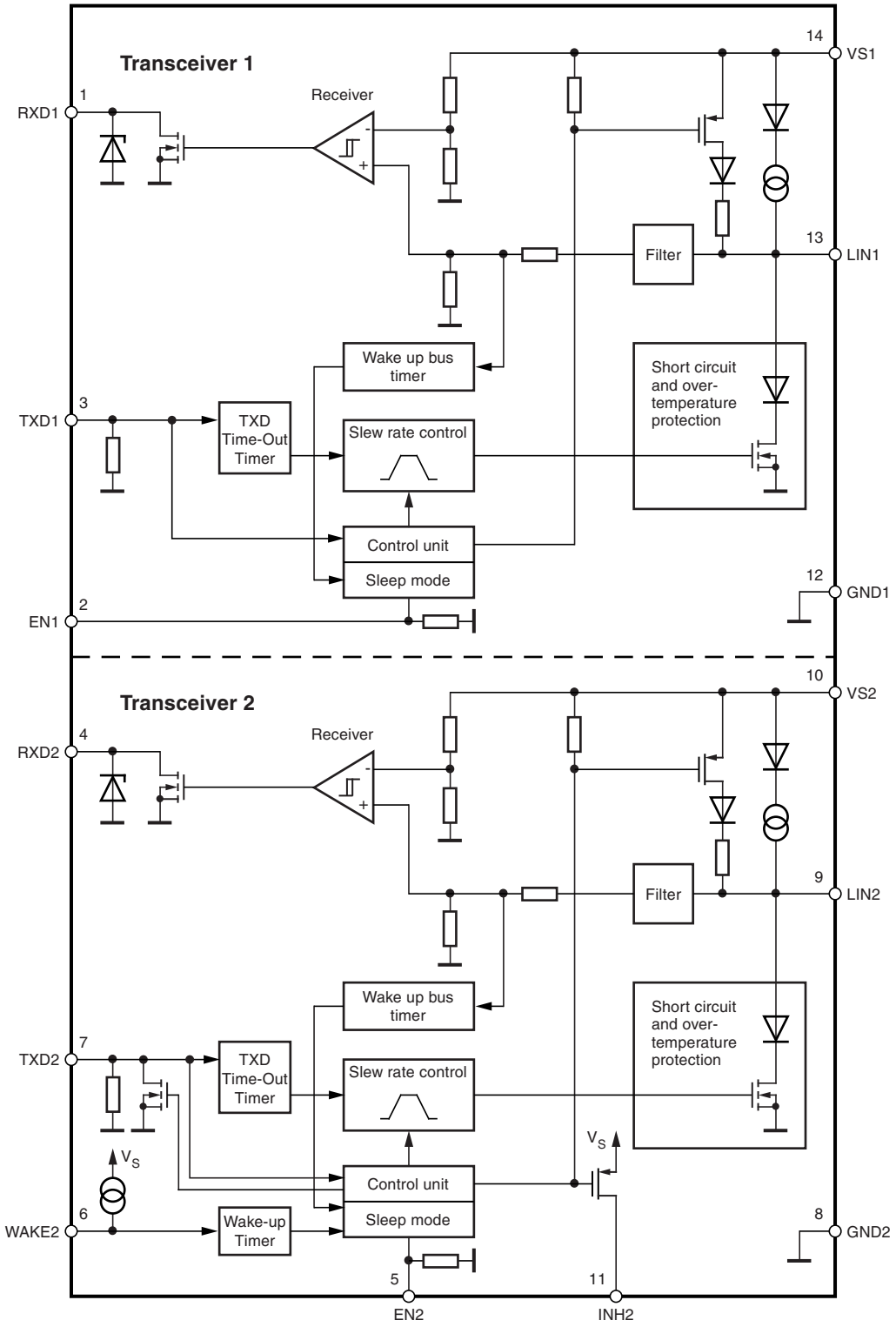
The Atmel® ATA6670 is a fully integrated Dual-LIN transceiver complying with the LIN specification 2.0, 2.1, and SAEJ2602-2. There are two completely independent and separated LIN transceivers integrated in one package (only the GND pins GND1 and GND2 are internally connected). Each of them interfaces with the LIN protocol handler and the physical layer.

The two LIN transceivers are nearly identical, the only difference is an additional wake input and an INH output at transceiver 2.

The device is designed to handle the low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN bus ensures secure data communication of up to 20Kbaud with an RC oscillator for protocol handling. Sleep mode guarantees minimal current consumption for each transceiver even in the case of a floating bus line or a short-circuit on the LIN bus to GND. The Atmel ATA6670 features advanced EMI and ESD performance.

9204C–AUTO–09/11

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning DFN14

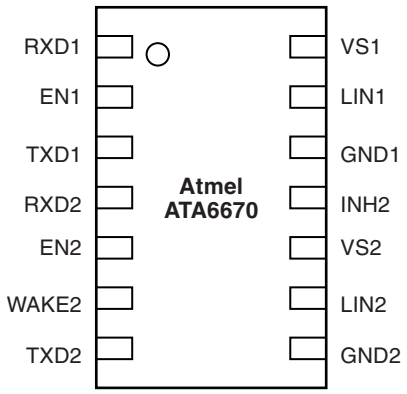


Table 2-1. Pin Description

Pin	Symbol	Function
1	RXD1	Receives data output 1 (open drain)
2	EN1	Enables normal mode 1. When the input is open or low, transceiver 1 is in sleep mode.
3	TXD1	Transmits data input 1, active low output (strong pull-down) after a local wake-up request
4	RXD2	Receives data output 2 (open drain)
5	EN2	Enables normal mode 2. When the input is open or low, transceiver 2 is in sleep mode.
6	WAKE2	High voltage input for local wake-up request. If not needed, connect directly to VS2
7	TXD2	Transmits data input 2, active low output (strong pull-down) after a local wake-up request
8	GND2	Ground 2
9	LIN2	LIN bus line 2 input/output
10	VS2	Battery supply 2
11	INH2	VS2- related high-side switch output for controlling an external load, such as a voltage divider
12	GND1	Ground 1
13	LIN1	LIN bus line 1 input/output
14	VS1	Battery supply 1

3. Functional Description

The functions described in the following text apply to each LIN transceiver. Therefore, if pin LIN is stated, this applies to each of the two receivers (LIN1 and LIN2), which work completely independently. The only internal connection is between GND1 and GND2. The functions only available at transceiver 2 are marked accordingly.

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent of higher LIN layers (e.g., the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes, which are based on older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

3.2 Supply Pin (VS)

Undervoltage detection is implemented to disable transmission if VS falls to a value below 5V in order to avoid false bus messages. After switching on VS, the corresponding transceiver switches to fail-safe mode. The supply current for each transceiver in sleep mode is typically 10µA.

3.3 Ground Pin (GND)

The Atmel ATA6670 does not affect the LIN bus in case of GND disconnection. It is able to handle a ground shift up to 11.5% of V_S.

3.4 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown and an internal pull-up resistor are implemented as specified for LIN 2.x. The voltage range is from –27V to +40V. This pin exhibits no reverse current from the LIN bus to V_S, even in case of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification. The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope-controlled. The output has a self-adapting short-circuit limitation; in other words, during current limitation, the current decreases in proportion to an increase in chip temperature.

Note: The internal pull-up resistor is only active in normal and fail-safe mode.

3.5 Input/ Pin (TXD)

In normal mode the TXD pin is the microcontroller interface to control the state of the LIN output. TXD must be at the low level in order to have a low LIN bus. If TXD is high, the LIN output transistor is turned off and the bus is in recessive state. The TXD pin is compatible with both a 3.3V and 5V supply.

3.6 TXD Dominant Time-out Function

The TXD input has an internal pull-down resistor. An internal timer prevents the bus line from being driven permanently in dominant state. If TXD is forced to low longer than t_{DOM} > 40ms, the LIN pin is switched off (recessive mode). To reset this mode, switch TXD to high (> 10µs) before switching LIN to dominant again.

3.7 Output Pin (RXD)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive) is reported by a high level at RXD, LIN low (dominant) is reported by a low voltage at RXD. The output is an open drain, therefore it is compatible with a 3.3V or 5V power supply. The AC characteristics are defined with a pull-up resistor of 5kΩ to 5V and a load capacitor of 20pF. The output is short current protected. In unpowered mode (V_S = 0V) RXD is switched off. For ESD protection a Zener diode is integrated with V_Z = 6.1V.

3.8 Enable Input Pin (EN)

This pin controls the operation mode of the LIN transceiver. If EN = 1, the LIN transceiver is in normal mode, with the transmission path from TXD to LIN and from LIN to RXD both active. At a falling edge on EN, while TXD is already set to high, the device is switched to sleep mode and no transmission is possible. In sleep mode, the LIN bus pin is connected to V_S with a weak pull-up current source. The device can transmit only after being woken up. During sleep mode the device is still supplied from the battery voltage. The supply current is typically 10µA. The pin EN provides a pull-down resistor in order to force the transceiver into sleep mode in case the pin is disconnected.

3.9 WAKE-up Input Pin (WAKE2, Only Available at Transceiver 2)

This pin is a high-voltage input used to wake up the transceiver 2 from sleep mode. It is usually connected to an external transistor or a switch to generate a local wake-up. A pull-up current source with typically –10µA is implemented as well as a debounce timer with a typical debounce time of 70µs.

Even if the WAKE2 pin is pulled to GND, it is possible to switch the transceiver 2 into sleep mode.

If a local wake-up is not needed in the application, pin WAKE2 can be connected directly to pin VS2.

3.10 INH Output Pin (INH2, only available at Transceiver 2)

This pin is used to control an external load or to switch the LIN master pull-up resistor on/off at pin LIN2. The inhibit pin provides an internal switch towards VS2 which is protected by temperature monitoring. If transceiver 2 is in normal or fail-safe mode, the inhibit high-side switch is turned on. When the transceiver 2 is in sleep mode, the inhibit switch is turned off, thus disabling the connected external devices.

A wake-up event on LIN2 or at pin WAKE2 puts the transceiver 2 into fail-safe mode and as a result the INH2 switches to the VS2 level. After a system power-up (VS2 rises from zero), the pin INH2 switches automatically to the VS2 level.

3.11 Operation Modes

1. Normal mode
   This is the normal transmitting and receiving mode. All features are available.
2. Sleep mode
   In this mode the transmission path is disabled and the device is in low power mode. Supply current from V_{Batt} is typically 10µA. A wake-up signal (either from the LIN bus or the WAKE2 input) is detected and switches the corresponding transceiver to fail-safe mode. If EN then switches to high, normal mode is activated. Input debounce timers at pin WAKE2 (t_{WAKE}), LIN (t_{BUS}) and EN ($t_{sleep,tnom}$) prevent undesirable wake-up events due to automotive transients or EMI. The internal termination between pin LIN and pin VS is disabled. Only a weak pull-up current (typical 10µA) between pin LIN and pin VS is present. Sleep mode can be activated independently of the current level on pin LIN.
3. Fail-safe mode
   At system power-up or after a wake-up event, the transceiver automatically switches to fail-safe mode. When VS2 exceeds 5V, the transceiver 2 switches the INH2 pin to the VS2 level. LIN communication is switched off. The microcontroller of the application then confirms normal mode by setting the EN pin to high.

Figure 3-1. Operating Modes

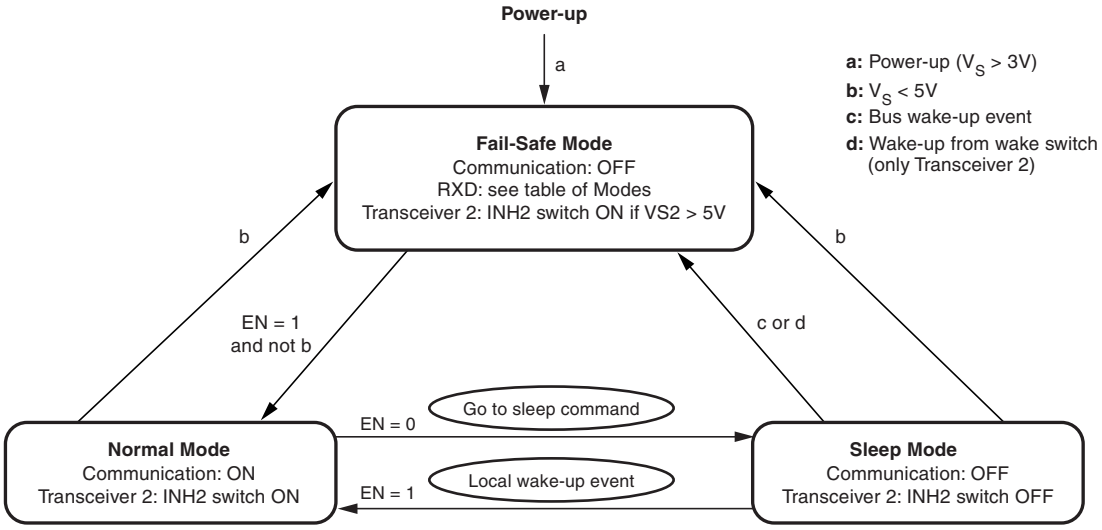


Table 3-1. Table of Modes

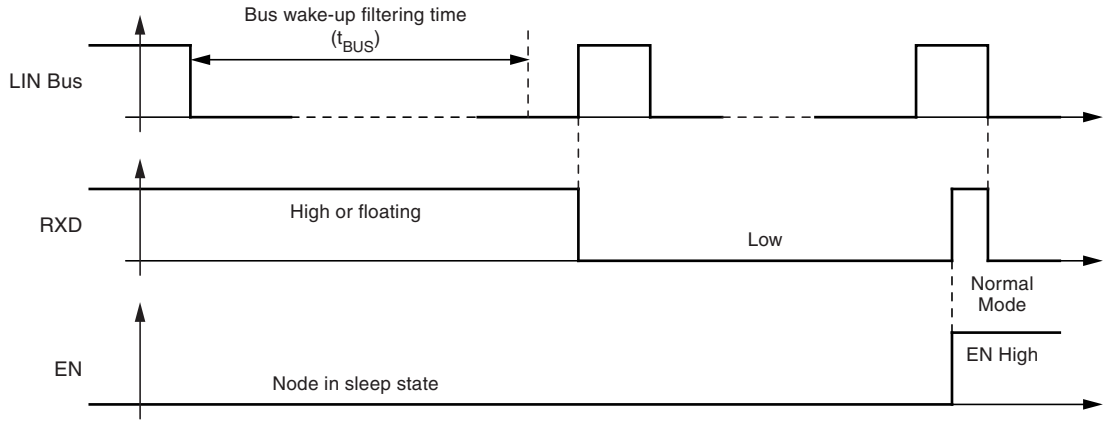
Operating Mode	Transceiver	RXD	LIN
Fail-safe	Off	High, except after wake-up	Recessive
Normal	On	LIN-depending	TXD-depending
Sleep	Off	High-ohmic	Recessive

3.12 Remote Wake-up via Dominant Bus State

A voltage lower than the LIN pre-wake detection VLINL at pin LIN activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at pin LIN, followed by a dominant bus level V_{BUSdom} maintained for a certain period of time (> t_{BUS}) and a rising edge at pin LIN results in a remote wake-up request. The transceiver switches to fail-safe mode, at transceiver 2 the INH2 output is activated (switches to VS2) and the internal termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (see Figure 3-2).

Figure 3-2. LIN Wake-up Waveform Diagram

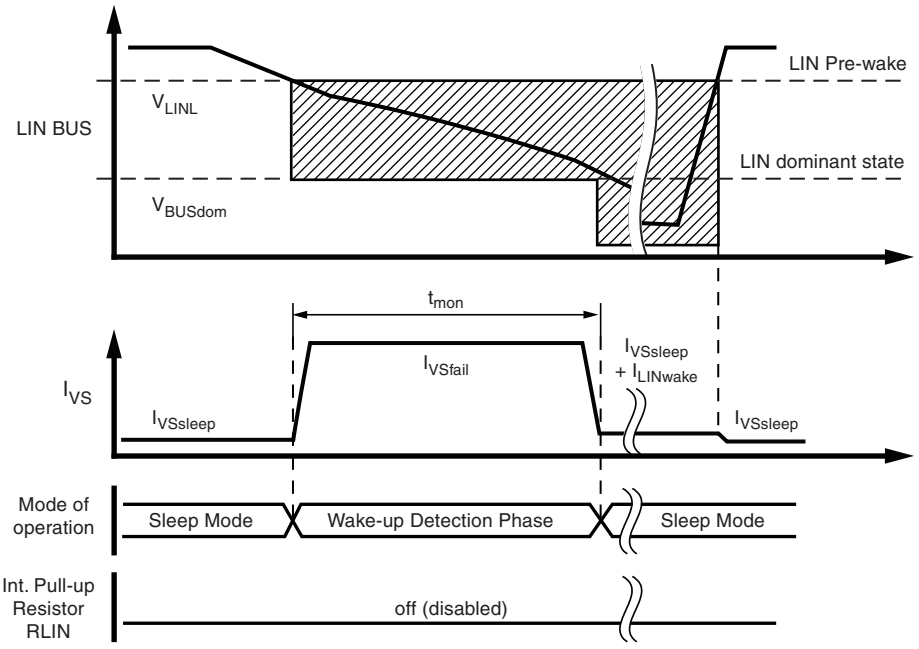


In sleep mode the device has a very low current consumption even during short-circuits or floating conditions on the bus. A floating bus can arise if the master pull-up resistor is missing, e.g., it is switched off when the LIN master is in sleep mode or even if the power supply of the master node is switched off.

In order to minimize the current consumption I_{VS} during voltage levels at the LIN pin below the LIN pre-wake threshold, the receiver is activated only for a specific time t_{mon}. If t_{mon} elapses while the voltage at the bus is lower than pre-wake detection low (V_{LINL}) and higher than the LIN-dominant level, the receiver is switched off again and the circuit reverts to sleep mode. The current consumption is then the result of $I_{VSsleep}$ plus $I_{LINwake}$. If a dominant state is reached on the bus, no wake-up will occur. Even if the voltage rises above the pre-wake detection high (V_{LINH}), the IC will stay in sleep mode (see Figure 3-3 on page 8).

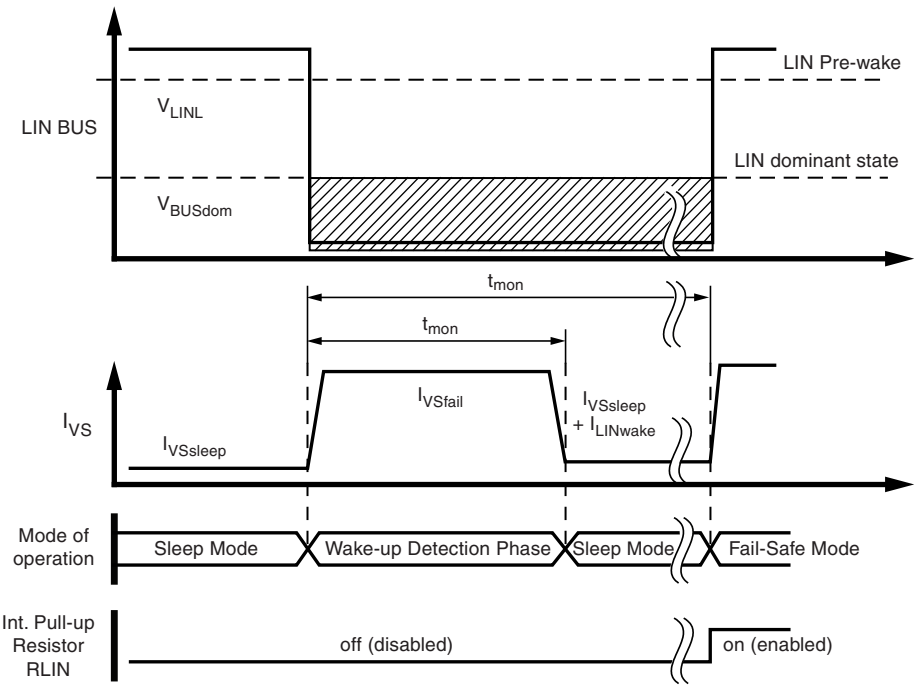
This means the LIN bus must be above the pre-wake detection threshold V_{LINH} for a few microseconds before a new LIN wake-up is possible.

Figure 3-3. Floating LIN Bus During Sleep Mode



If the Atmel® ATA6670 is in sleep mode and the voltage level at the LIN is in dominant state ($V_{LIN} < V_{BUSdom}$) for a period of time exceeding t_{mon} (during a short circuit at LIN, for example), the IC switches back to sleep mode. The VS current consumption then consists of $I_{VSsleep}$ plus $I_{LINWAKE}$. After a positive edge at pin LIN the IC switches directly to fail-safe mode (see Figure 3-4).

Figure 3-4. Short-circuit to GND on the LIN Bus During Sleep Mode

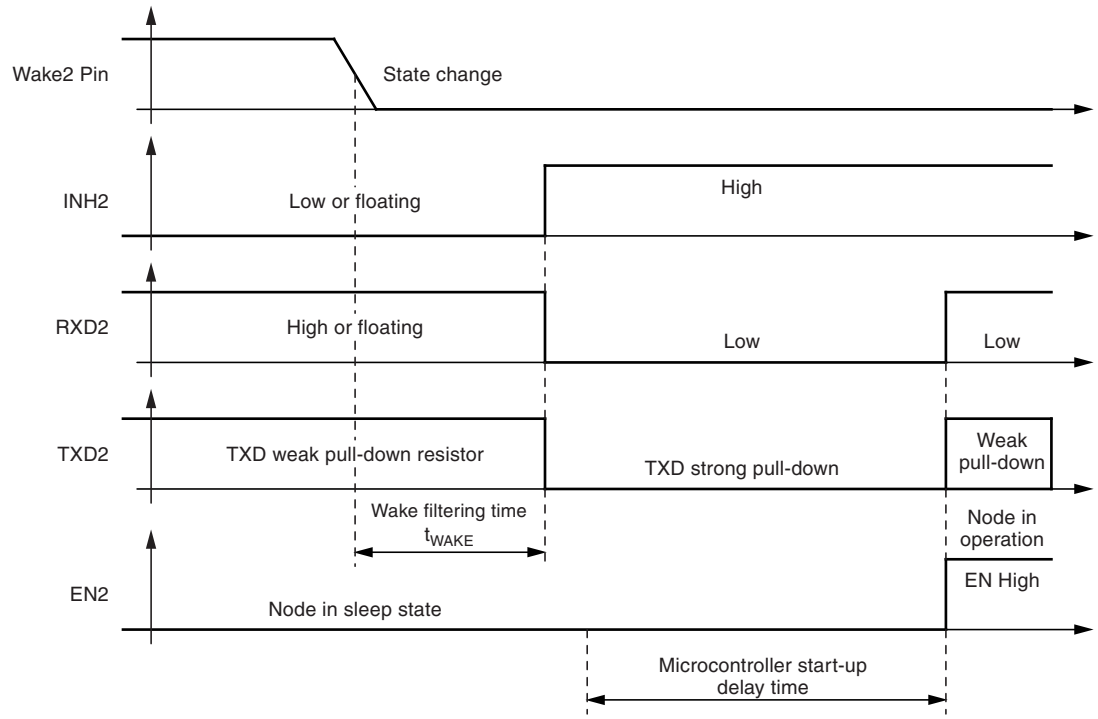


3.13 Local WAKE-up via Pin WAKE2 (Only Available at Transceiver 2)

A falling edge at pin WAKE2 followed by a low level maintained for a certain period of time (> t_{WAKE}) results in a local wake-up request. According to ISO 7637, the wake-up time ensures that no transients create a wake-up. The transceiver 2 then switches to fail-safe mode. Pin INH2 is activated (switches to VS2) and the internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at pin RXD for interrupting the microcontroller and by a strong pull-down at pin TXD. (see Figure 3-5).

The voltage threshold for a wake-up signal is 3V below the VS2 voltage with an output current of typically –3µA. Even in the case of a continuos low at pin WAKE2 it is possible to switch the transceiver 2 into sleep mode via a low level at pin EN2. The transceiver 2 will remain in sleep mode for an unlimited time. To generate a new wake-up at pin WAKE2, a high signal for > 6µs is required. A negative edge then restarts the wake-up filtering time.

Figure 3-5. LIN Transceiver 2: Wake-up from Wake-up Switch (WAKE2)



3.14 Wake- up Source Recognition (Only available at Transceiver 2)

Transceiver 2 can distinguish between a local wake-up request at pin WAKE2 and a remote wake-up request via LIN 2. The wake-up source can be read at pin TXD in fail-safe mode. If an external pull up resistor (typ. 5kΩ) has been added on pin TXD2 to the power supply of the microcontroller, a high level indicates a remote wake-up request (weak pull down at pin TXD2), a low level indicates a local wake-up request (strong pull down at pin TXD2).

The wake-up request flag (indicated at pin RXD2) as well as the wake-up source flag (indicated at pin TXD2) are immediately reset if the microcontroller sets pin EN2 to high (see Figure 3-5 on page 9).

3.15 Fail-safe Features

- During a short-circuit at LIN to $V_{Battery}$, the output limits the output current to IBUS_LIM. Due to the power dissipation, the chip temperature exceeds T_{off}, and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys} it switches the output on again.
- During a short-circuit from LIN to GND the transceiver can be switched into sleep mode and even in this case the current consumption is lower than 45µA. If the short-circuit disappears, the transceiver starts with a remote wake-up.
- If a transceiver is in sleep mode and a floating condition occurs on the bus, the transceiver automatically switches back to sleep mode, thus decreasing current consumption to less than 45µA in this case.
- The reverse current is < 2µA at pin LIN during loss of V_{BAT}; this is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- Pin EN provides a pull-down resistor to force the transceiver into sleep mode if EN is disconnected.
- Pin RXD is set to floating if V_{BAT} is disconnected.
- Pin TXD provides a pull-down resistor to provide a static low if TXD is disconnected.
- After switching the LIN transceiver into Normal Mode the TXD pin must be pulled to high longer than 10µs in order to activate the LIN driver. This feature prevents the bus from being driven into dominant state when the LIN transceiver is switched into Normal Mode and TXD is low.
- The INH2 output transistor at transceiver 2 is protected by temperature monitoring

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
V_{S1}, V_{S2} - Continuous supply voltage		–0.3		+40	V
WAKE2 - DC and transient voltage (with 2.7kΩ serial resistor) - Transient voltage according to ISO7637 (coupling 1nF)		 –27 –150		 +40 +100	 V V
Logic pins (RXD1, RXD2, TXD1, TXD2, EN1, EN2)		–0.3		+5.5	V
LIN1, LIN2 - DC voltage - Transient voltage according to ISO7637 (coupling 1nF)		 –27 –150		 +40 +100	 V V
INH2 - DC voltage		–0.3		V_{S2} + 0.3	V
ESD according to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2 - Pin VS1, VS2, LIN1, LIN2 to GND - Pin WAKE2 (2.7kΩ serial resistor)		 ±8 ±6			 KV KV
ESD HBM following STM5.1 with 1.5kΩ / 100pF - Pin VS1, VS2, LIN1, LIN2, WAKE2, INH2 to GND		 ±6			 KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		 ±3			 KV
CDM ESD STM 5.3.1		±750			V
Machine model ESD AEC-Q100-Rev.F (003)		±200			V
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_{stg}	–55		+150	°C

5. Thermal Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction to heat slug	R_{thJC}		8		K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB according to Jedec	R_{thJA}		45		K/W
Thermal shutdown	T_{off}	150	165	180	°C
Thermal shutdown hysteresis	T_{hys}	5	10	20	°C

6. Electrical Characteristics

5V < V_S < 27V, T_j = –40°C to +150°C; the values below are valid for each of the two nearly identical integrated LIN transceivers unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**V_S Pin**								
1.1	DC voltage range nominal		VS	V_S	5	13.5	27	V	A
1.2	Supply current in sleep mode	Sleep mode $V_{LIN} > V_S - 0.5V$ V_S < 14V	VS	$I_{VSsleep}$		10	20	µA	A
		Sleep mode, bus shorted to GND V_{LIN} = 0V V_S < 14V	VS	$I_{VSsleep\_sc}$		23	45	µA	A
1.3	Supply current in normal mode	Bus recessive V_S < 14V	VS	I_{VSrec}		0.9	1.3	mA	A
1.4		Bus dominant V_S < 14V Total bus load > 500Ω	VS	I_{VSdom}		1.2	2	mA	A
1.5	Supply current in fail-safe mode	Bus recessive V_S < 14V	VS	I_{VSfail}	0.5		1.1	mA	A
1.6	V_S undervoltage threshold on		VS	V_{Sth}	4		4.95	V	A
1.7	V_S undervoltage threshold off		VS	V_{Sth}	4.05		5	V	A
1.8	V_S undervoltage threshold hysteresis		VS	V_{Sth_hys}	50		500	mV	A
2	**RXD Output Pin (Open Drain)**								
2.1	Low-level output sink current	Normal mode V_{LIN} = 0V, V_{RXD} = 0.4V	RXD	I_{RXDL}	1.3	2.5	8	mA	A
2.2	RXD saturation voltage	5-kΩ pull-up resistor to 5V	RXD	$Vsat_{RXD}$			0.4	V	A
2.3	High-level leakage current	Normal mode V_{LIN} = V_{BAT}, V_{RXD} = 5V	RXD	I_{RXDH}	–3		+3	µA	A
2.4	ESD Zener diode	I_{RXD} = 100µA	RXD	VZ_{RXD}	5.8		8.6	V	A
3	**TXD Input/Output Pin**								
3.1	Low-level voltage input		TXD	V_{TXDL}	–0.3		+0.8	V	A
3.2	High-level voltage input		TXD	V_{TXDH}	2		7	V	A
3.3	Pull-down resistor	V_{TXD} = 5V	TXD	R_{TXD}	125	250	600	kΩ	A
3.4	Low-level leakage current	V_{TXD} = 0V	TXD	I_{TXD_leak}	–3		+3	µA	A
3.5	Low-level output sink current (only available at transceiver 2)	Transceiver 2: fail-safe mode, local wake-up V_{TXD2} = 0.4V V_{LIN2} = V_{BAT}	TXD2	I_{TXD2}	1.3	2.5	8	mA	A
4	**EN Input Pin**								
4.1	Low-level voltage input		EN	V_{ENL}	–0.3		+0.8	V	A
4.2	High-level voltage input		EN	V_{ENH}	2		7	V	A
4.3	Pull-down resistor	V_{EN} = 5V	EN	R_{EN}	125	250	600	kΩ	A
4.4	Low-level input current	V_{EN} = 0V	EN	I_{EN}	–3		+3	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = –40°C to +150°C; the values below are valid for each of the two nearly identical integrated LIN transceivers unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5	**INH 2 Output Pin (Only Available at Transceiver 2)**								
5.1	High-level voltage	Normal or fail-safe mode I_{INH2} = –15mA	INH2	V_{INH2H}	V_{S2} – 0.75		V_{S2}	V	A
5.2	Switch-on resistance between VS2 and INH2	Normal or fail-safe mode	INH2	R_{INH2}		30	50	Ω	A
5.3	Leakage current	Transceiver 2 in sleep mode V_{INH2} = 0V/27V, V_{S2} = 27V	INH2	I_{INH2L}	–3		+3	µA	A
6	**WAKE2 Input Pin (only available at Transceiver 2)**								
6.1	High-level input voltage		WAKE2	V_{WAKE2H}	V_{S2} – 1V		V_{S2} + 0.3V	V	A
6.2	Low-level input voltage	I_{WAKE2} = typically –3µA	WAKE2	V_{WAKE2L}	–1V		V_{S2} – 3.3V	V	A
6.3	Wake2 pull-up current	V_{S2} < 27V	WAKE2	I_{WAKE2}	–30	–10		µA	A
6.4	High-level leakage current	V_{S2} = 27V, V_{WAKE2} = 27V	WAKE2	I_{WAKE2}	–5		+5	µA	A
7	**LIN Bus Driver**								
7.1	Driver recessive output voltage	R_{LOAD} = 500Ω/1kΩ	LIN	V_{BUSrec}	0.9 × V_S		V_S	V	A
7.2	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VS} = 7V, R_{load} = 500Ω	LIN	$V_{\_LoSUP}$			1.2	V	A
7.3	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VS} = 18V, R_{load} = 500Ω	LIN	$V_{\_HiSUP}$			2	V	A
7.4	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VS} = 7V, R_{load} = 1000Ω	LIN	$V_{\_LoSUP\_1k}$	0.6			V	A
7.5	Driver dominant voltage $V_{BUSdom\_DRV\_HiSUP}$	V_{VS} = 18V, R_{load} = 1000Ω	LIN	$V_{\_HiSUP\_1k\_}$	0.8			V	A
7.6	Pull-up resistor to V_S	The serial diode is mandatory	LIN	R_{LIN}	20	30	47	kΩ	A
7.7	Voltage drop at the serial diodes	In pull-up path with R_{slave} $I_{SerDiode}$ = 10mA	LIN	$V_{SerDiode}$	0.4		1.0	V	D
7.8	LIN current limitation V_{BUS} = V_{BAT_max}		LIN	I_{BUS_LIM}	40	120	200	mA	A
7.9	Input leakage current at the receiver, including pull-up resistor as specified	Input leakage current driver off V_{BUS} = 0V, V_S = 12V	LIN	$I_{BUS\_PAS\_dom}$	–1			mA	A
7.10	Leakage current LIN recessive	Driver off 8V < V_{BAT} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{BAT}$	LIN	$I_{BUS\_PAS\_rec}$		10	20	µA	A
7.11	Leakage current at ground loss; control unit disconnected from ground; loss of local ground must not affect communication in the residual network	GND_{Device} = V_S V_{BAT} =12V 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_Gnd}$	–10	+0.5	+10	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = –40°C to +150°C; the values below are valid for each of the two nearly identical integrated LIN transceivers unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.12	Leakage current at loss of battery, node has to sustain the current that can flow under this condition, bus must remain operational under this condition	V_{BAT} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V	LIN	$I_{BUS\_NO\_Bat}$		0.1	2	µA	A
7.13	Capacitance on pin LIN to GND		LIN	C_{LIN}			20	pF	D
8	**LIN Bus Receiver**								
8.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec}) / 2	LIN	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	A
8.2	Receiver dominant state	V_{EN} = 5V	LIN	V_{BUSdom}	–27		0.4 × V_S	V	A
8.3	Receiver recessive state	V_{EN} = 5V	LIN	V_{BUSrec}	0.6 × V_S		40	V	A
8.4	Receiver input hysteresis	V_{HYS} = V_{th_rec} – V_{th_dom}	LIN	V_{BUShys}	0.028 × V_S	0.1 × V_S	0.175 × V_S	V	A
8.5	Pre-wake detection LIN high-level input voltage		LIN	V_{LINH}	V_S – 2V		V_S + 0.3V	V	A
8.6	Pre-wake detection LIN Low-level input voltage	Switches the LIN receiver on	LIN	V_{LINL}	–27V		V_S – 3.3V	V	A
8.7	LIN pre-wake pull-up current	V_S < 27V V_{LIN} = 0V	LIN	$I_{LINWAKE}$	–30	–10		µA	A
9	**Internal Timers**								
9.1	Dominant time for wake-up via LIN bus	V_{LIN} = 0V	LIN	t_{BUS}	30	90	150	µs	A
9.3	Time delay for mode change from fail-safe mode to normal mode via pin EN	V_{EN} = 5V	EN	t_{norm}	2	7	15	µs	A
9.4	Time delay for mode change from normal mode into sleep mode via pin EN	V_{EN} = 0V	EN	t_{sleep}	7	12	20	µs	B
9.5	TXD dominant time out time	V_{TXD} = 0V	TXD	t_{dom}	27	55	70	ms	A
9.6	Monitoring time for wake-up over LIN bus		LIN	t_{mon}	6	10	15	ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = –40°C to +150°C; the values below are valid for each of the two nearly identical integrated LIN transceivers unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10	**LIN Bus Driver AC Parameter with Different Bus Loads** Load 1 (small): 1nF, 1kΩ; Load 2 (large): 10nF, 500Ω; R_{RXD} = 5kΩ; C_{RXD} = 20pF; Load 3 (medium): 6.8nF, 660Ω characterized on samples; 10.1 and 10.2 specifies the timing parameters for proper operation at 20Kbit/s, 10.3 and 10.4 at 10.4Kbit/s.								
10.1	Duty cycle 1	$TH_{Rec(max)}$ = 0.744 × V_S $TH_{Dom(max)}$ = 0.581 × V_S V_S = 7.0V to 18V t_{Bit} = 50µs D1 = $t_{bus\_rec(min)}$ / (2 × t_{Bit})	LIN	D1	0.396				A
10.2	Duty cycle 2	$TH_{Rec(min)}$ = 0.422 × V_S $TH_{Dom(min)}$ = 0.284 × V_S V_S = 7.0V to 18V t_{Bit} = 50µs D2 = $t_{bus\_rec(max)}$ / (2 × t_{Bit})	LIN	D2			0.581		A
10.3	Duty cycle 3	$TH_{Rec(max)}$ = 0.778 × V_S $TH_{Dom(max)}$ = 0.616 × V_S V_S = 7.0V to 18V t_{Bit} = 96µs D3 = $t_{bus\_rec(min)}$ / (2 × t_{Bit})	LIN	D3	0.417				A
10.4	Duty cycle 4	$TH_{Rec(min)}$ = 0.389 × V_S $TH_{Dom(min)}$ = 0.251 × V_S V_S = 7.0V to 18V t_{Bit} = 96µs D4 = $t_{bus\_rec(max)}$ / (2 × t_{Bit})	LIN	D4			0.590		A
11	**Receiver Electrical AC Parameters of the LIN Physical Layer** LIN receiver, RXD load conditions: C_{RXD} = 20pF, $R_{pull-up}$ = 5kΩ								
11.1	Propagation delay of receiver (see Figure 6-1 on page 16)	t_{rec_pd} = max(t_{rx_pdr} , t_{rx_pdf}) V_S = 7.0V to 18V	RXD	t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf} V_S = 7.0V to 18V	RXD	t_{rx_sym}	–2		+2	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 6-1. Definition of Bus Timing Parameter

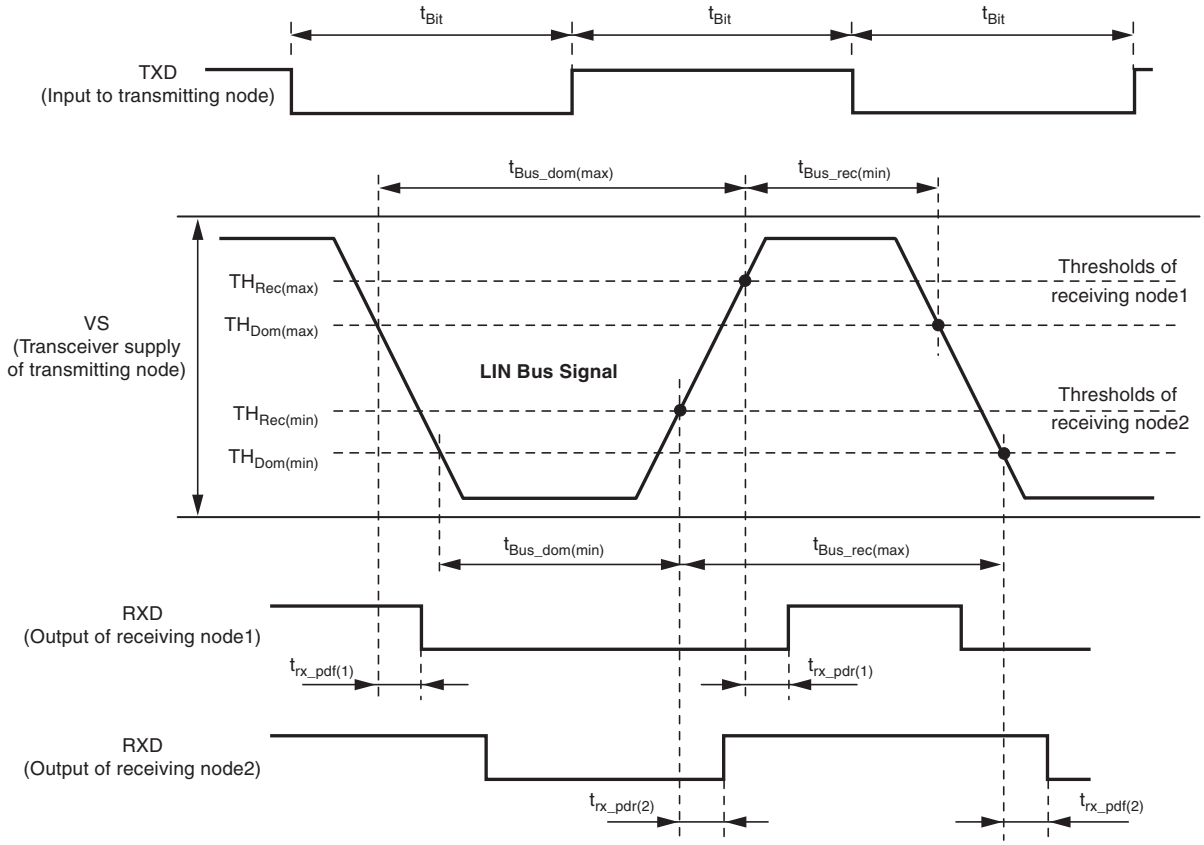


Figure 6-2. Typical Application Circuit

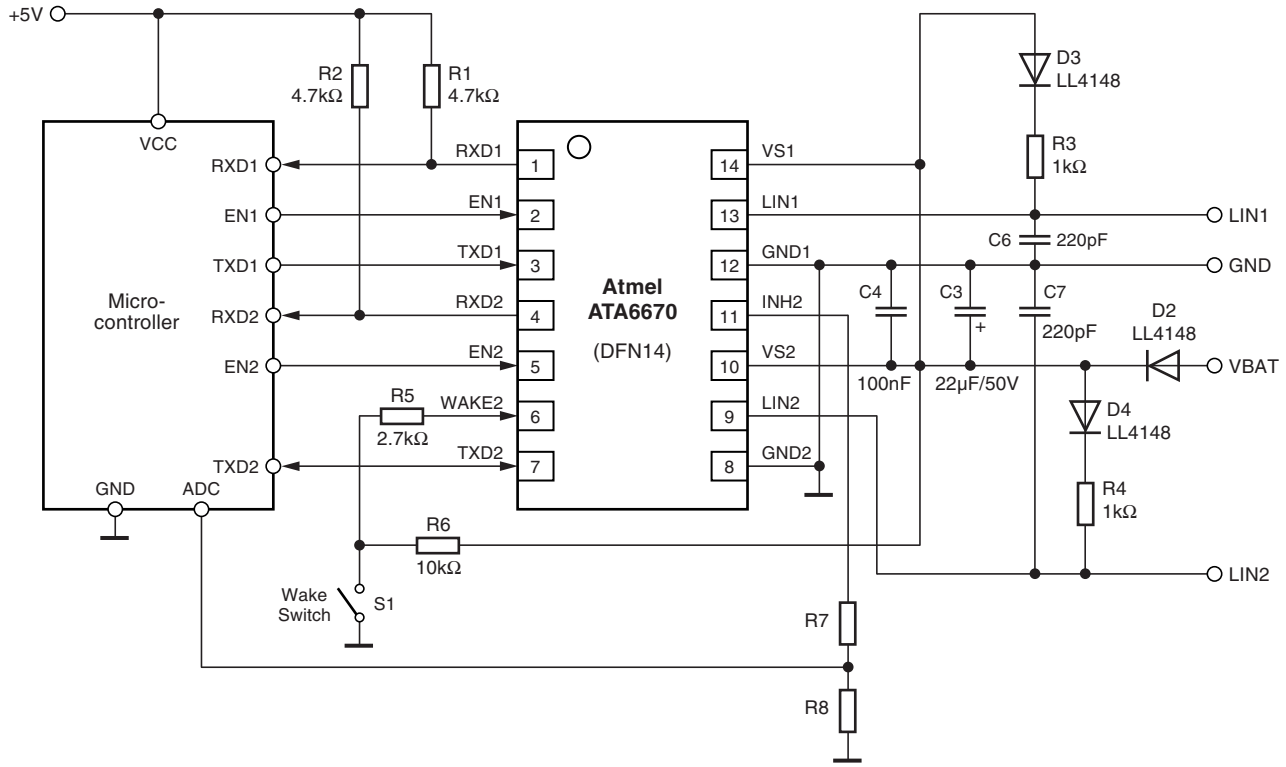
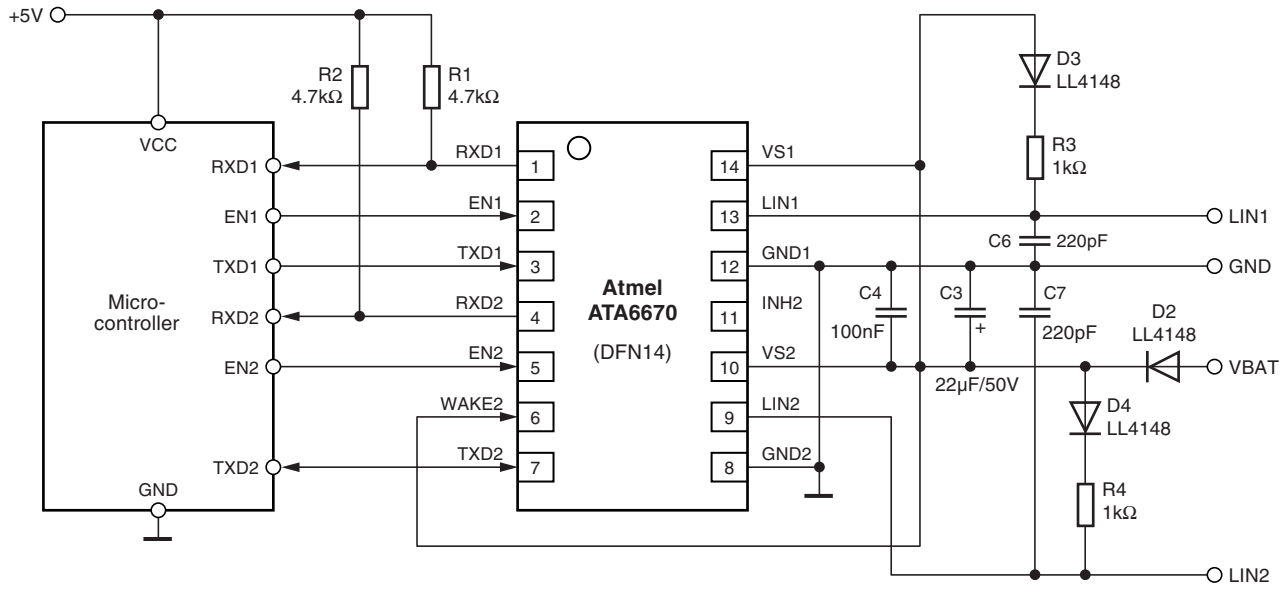


Figure 6-3. Application with Minimum External Devices: INH2 Output and WAKE2 Input Not Used

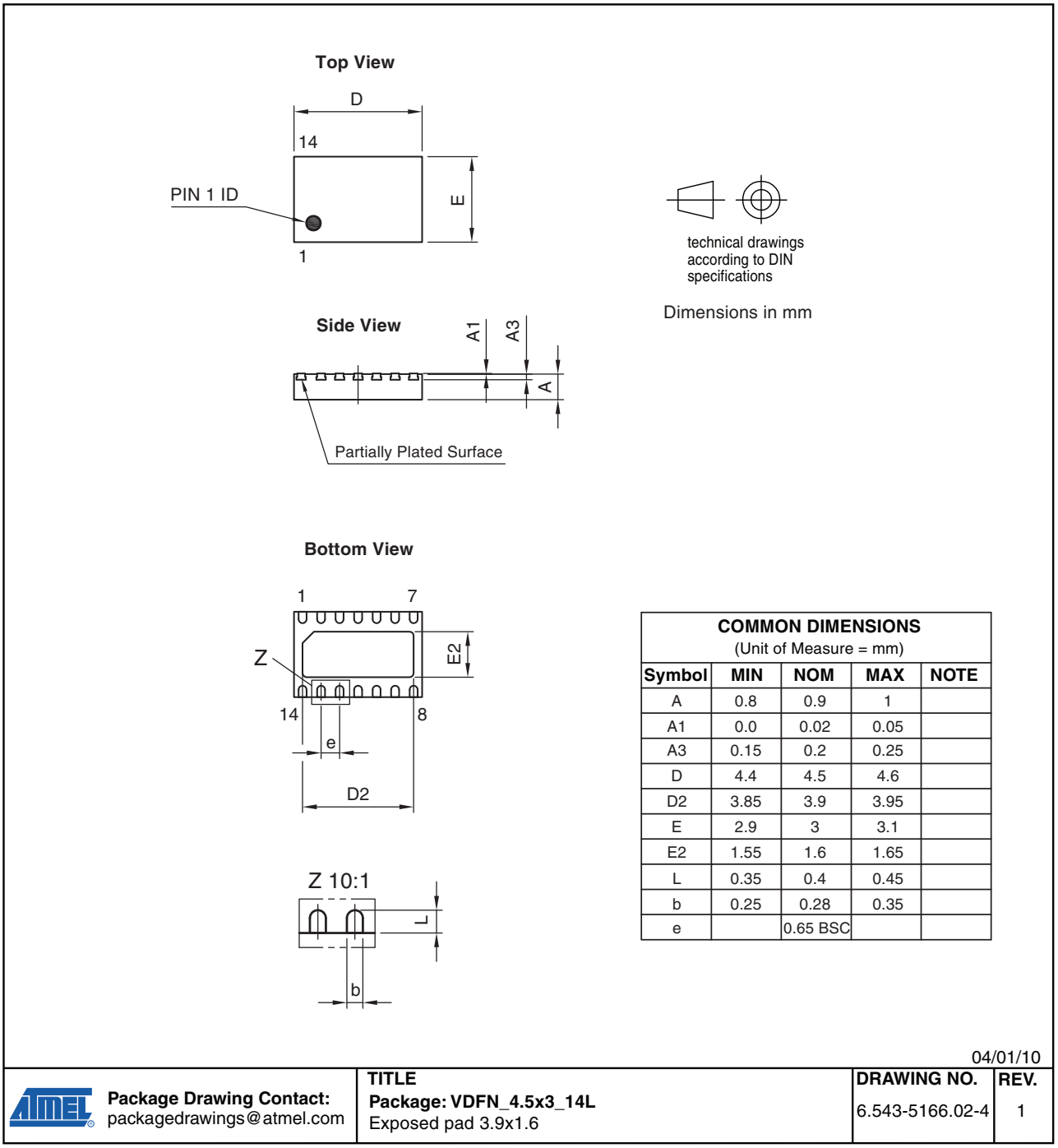


7. Ordering Information

Extended Type Number	Package	Remarks
ATA6670-FFQW	DFN14	LIN Transceiver, Pb-free, 6k, taped and reeled.

8. Package Information

Figure 8-1. DFN14



COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	0.8	0.9	1	
A1	0.0	0.02	0.05	
A3	0.15	0.2	0.25	
D	4.4	4.5	4.6	
D2	3.85	3.9	3.95	
E	2.9	3	3.1	
E2	1.55	1.6	1.65	
L	0.35	0.4	0.45	
b	0.25	0.28	0.35	
e		0.65 BSC		

04/01/10

Package Drawing Contact: packagedrawings@atmel.com	TITLE	DRAWING NO.	REV.
	Package: VDFN_4.5x3_14L Exposed pad 3.9x1.6	6.543-5166.02-4	1

9. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9204C-AUTO-09/11	• Section 7 “Ordering Information” on page 18 changed
9204B-AUTO-03/11	• Figure 1-1 “Block Diagram” on page 2 changed • Section 3.15 “Fail-safe Features” on page 10 changed

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